RESEARCH ARTICLE

Fabrication of n^+-poly-Si/p^+-c-Si tunnel diode using Low-pressure Chemical Vapor Deposition for Photovoltaic Applications

*Vineet Kumar Singh**

In this paper, an n^+-poly-silicon/p^+-crystalline-silicon tunnel diode has been fabricated and characterized. The n^+ poly-silicon layer is deposited by the low-pressure chemical vapor deposition method, while a diffusion furnace is used for boron diffusion in crystalline silicon. Scanning electron microscopy and X-ray diffraction pattern have been used for structural characterization. Hall measurement and current-voltage characteristics have been used for carrier density, mobility, current density, and contact resistance measurement. Hall measurement reveals the carrier density of ~10^{19} cm^{-3} in phosphorus-doped poly-silicon tunnel layer with mobility of ~5.4 cm^2 V^{-1}-s^{-1}. The current-voltage characteristics of the tunnel diode show the current density of ~10^3 Ampere/cm^2 at a voltage of 0.1 Volt. Using tunnel diode, an n^+-poly-Si/p^+-c-Si/n-c-Si/n^+-c-Si structure has been fabricated for photovoltaic application. This structure generates a current density of ~17.9 mA/cm^2 and a voltage of 601 mV for a 195±10 nm thick doped poly-silicon layer. Further, to improve the solar cell's performance, a thin layer of poly-silicon has been used.

Introduction

Efficiency for crystalline silicon (c-Si) solar cells has stabilized at 26.7%, very close to its theoretical limit of 29.56% [**1-4**]. Tandem solar cells with two absorber layers have the potential to yield efficiency beyond 40% [**5**]. Polycrystalline silicon-based tunnel diodes play an essential role in the tandem solar cell [**6-9**]. Mailoa *et al.* reported the mixed-phase (amorphous + polycrystalline) silicon /crystalline silicon tunnel diode in the 2-terminal perovskite/silicon tandem solar cell using plasma-enhanced chemical vapor deposition (PECVD) method in 2015 [**9**]. However, the mixed-phase silicon tunnel layer fabricated through the PECVD method requires a complicated multi-step process [**9**]. First, a thin layer (2-3 nm) of intrinsic amorphous silicon is deposited at 250 °C to avoid the inter-diffusion of dopants as well as to reduce the interface recombination loss [**9**]. Next, a doped amorphous silicon layer is deposited at 250 °C. Finally, the films are annealed at ~680 °C to activate the dopants [**9**].

Römer *et al.*, also demonstrate the applicability of poly-silicon/mono-silicon tunnel junctions on solar cells and studied the influence of the interfacial oxide on the contact resistance and recombination [**10**]. Low-pressure chemical vapor deposition (LPCVD) was used only for intrinsic poly-silicon deposition during fabrication. The diffusion process was further used to dope the intrinsic poly-Si [10]. Römer *et al.*, reported the emitter saturation current density of 5fA/cm² for n^+-poly- Si/n-c-Si/ n^+-poly-Si test structure and further evaluated the contact resistance of 0.012 ± 0.007 Ω-cm^2 for Al/ITO/poly-Si/SiO_x/c-Si test structure using an ultra-thin layer (~1.2 nm) of SiO_x [**10**]. Next, Römer *et al.*, also estimated ~0.16% overall loss in the efficiency for the 0.1 Ω-cm^2 contact resistance at 42 mA-cm^{-2} short circuit current density and 10 fA-cm^{-2} emitter saturation current density [**11**].

R. Peibst *et al.*, reported the passivating n^+-type poly-silicon on oxide (POLO) contacts and evaluated relative junction resistance (~0.013) for p^+-poly-Si/n^+-poly-Si/SiO_x/n-c-Si/SiO_x/n^+-poly-Si/p^+-poly-Si structure [**12**]. Doped poly-silicon layers (p^+-poly-Si/n^+-poly-Si) have been used as a tunnel diode in the device structure rather than poly-silicon/c-Si junctions reported by Römer *et al.*, and Mailoa *et al.*, [**9,12**]. R. Peibst *et al.*, estimated the implied voltage of 718 mV for POLO-PERC (passivated emitter and rear contact) cell under one sun using poly-Si tunnel diodes [**12**]. Recently, C Luderer *et al.*, reported the tunnel oxide passivated contact (TOPCon) along with p^+/n^+poly-Si as tunnel diode using the PECVD process to estimate the combined resistance [**13**]. The estimated combined junction resistance for the p^+/n^+ poly-Si/SiO_x structure was <10 mΩ-cm^2 and implied open-circuit voltage was 726 mV [**13**].

Department of Physics, DDU Gorakhpur University, Gorakhpur-273009, India
*Corresponding author:
E-mail: 1vineetkumarsingh@gmail.com

DOI: 10.5185/amlett.2022.021693

Deposition of doped poly-silicon is a well-established commercial technique that can be done at a large-scale using low-pressure CVD in a single step rather than multiple steps used in PECVD [**14**]. The poly-Si tunnel junction fabricated by LPCVD is electrically and optically stable at 500 °C [**9**]. But the challenge is the deposition of highly doped, very thin layers with low absorption losses for photovoltaic application.

In this work, a poly-silicon/c-silicon tunnel diode is demonstrated and characterized. The poly-silicon layer is deposited by the low-pressure CVD method. The impact of poly-silicon thickness on the electrical and optical properties of the n^+-poly-Si/p^+-c-Si/n-c-Si/n^+-c-Si structure is also quantified. A tunnel layer is integrated with titanium oxide (TiO_2) film to establish the suitability of tandem cell (ETL/perovskite/TiO_2/n^+-poly-Si/p^+-c-Si/n-c-Si/n^+-c-Si).

However, the complete tandem cell has not been fabricated in this work.

Experimentaldetails

Fabrication of n^+-poly-Si/p^{++}-c-Si tunnel diode

Fabrication starts with a highly doped p-type float-zone 500 μm thick Si (100) wafer (~0.001 Ω-cm). The details of the complete fabrication steps are given in **Fig. 1(A)**. Initially, wafers were cleaned using RCA1 and RCA2 recipes for 15 minutes, followed by 1:100 HF etch for 1 minute to remove the chemical oxide. Further, using thermal oxidation at 1100 °C in a First Nano ET600 furnace, 1080 nm thick oxide was grown. Next, the top SiO_2 layer was etched by a buffered oxide etch (BOE) solution to diffuse the boron and generate a p^+ diffused region. A dielectric borosilicate glass formed during the boron diffusion process, which was further etched by BOE solution. Next, backside oxide is etched by 1:100 HF solutions. Now, RCA cleaned boron-doped wafers inserted in a First Nano ET600 LPCVD chamber for phosphorus-doped poly-silicon deposition at 620 °C. The required electrode patterns were deposited using optical lithography and the lift-off process. To ensure the ohmic contact, forming gas annealing was performed at 400 °C for 15 minutes. The device was kept small (**Fig. 1(B)**), 60μm×60μm, so that the measured currents remained within the measuring instrument limit (1A). Finally, two devices were fabricated: (1) control device without tunnel diode (just substrate, Al/p^{++} -Si/Al) and (2) test structure with the n^+-poly-Si/p^{++}-c-Si tunnel diode.

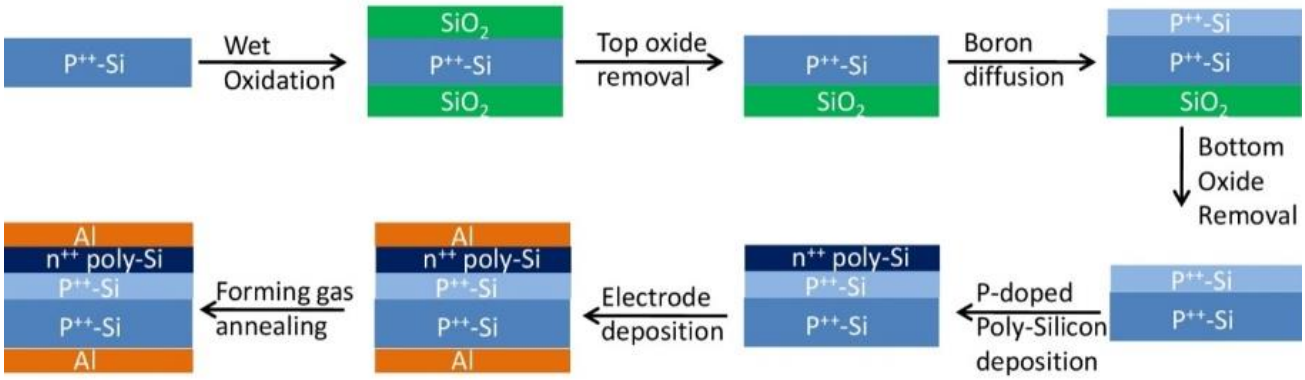

Fig. 1(A) Fabrication steps of the tunnel diode test structure.

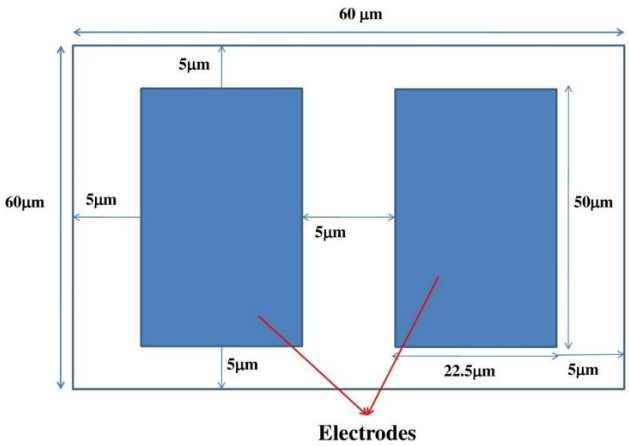

Fig. 1(B) Tunnel diode test structure area is 60μm × 60μm, while top electrode dimension is 50μm×22.5μm.

Fabrication of n^+-poly-Si/p^+-c-Si/n-c-Si/n^+-c-Si structure with and without TiO_2

The n^+-poly-Si/p^+-c-Si/n-c-Si/n^+-c-Si structure was fabricated on n-type float-zone 500 μm thick Si (100) wafers (1-10 Ω-cm) rather than earlier discussed highly doped p-type float-zone Si wafer. The complete process flow to fabricate the device is given in **Fig. 2**. Wafers were cleaned using the well-known RCA recipe for 15 minutes, followed by 1:100 HF etch for 1 minute to remove the chemical oxide. Next, a 1080 nm thick SiO_2 layer is grown at 1100 °C in a First Nano ET600 furnace. The bottom SiO_2 layer was etched by a buffered oxide etch (BOE) solution. Next, a blanket back-surface field (BSF) was formed by diffusing phosphorus using $POCl_3$ by a two-step process: pre-deposition for 15 minutes at 850 °C followed by a drive-in for 15 minutes at 950 °C. During

the phosphorus diffusion process a dielectric phosphorus silicate glass (PSG) layer was formed which was etched by BOE. Further, a 1µm thick PECVD SiO_2 was deposited using an Oxford Plasmalab100 system, to act as a mask for the subsequent emitter formation. The p+/n emitter junction was fabricated by boron diffusion using B_2H_6 gas by a two-step process: pre-deposition for 10 minutes at 900 °C followed by a drive-in for 8 minutes at 1100 °C in active area of 1 cm^2. During boron diffusion, a dielectric borosilicate glass layer was formed which was etched by BOE. Phosphorus doped poly-silicon layer was deposited on top of the emitter at 620°C in a First Nano ET600 LPCVD. A TiO_2 film (45±2 nm) was deposited using a BENEQ TFS200 atomic layer deposition (ALD) system at 250 °C for 1025 cycles. The TiO_2 on the bottom surface was etched using 1:10 hydrofluoric acid. Finally, aluminum back and front electrodes were deposited using a Techport electron-beam evaporator. The front aluminum electrode was patterned into a grid by lithography and lift-off process. The active area (including the top electrodes area) of the cell is 1cm^2. Devices were annealed in forming gas (N_2:H_2::10:1) at 350 °C for 15 minutes to ensure the proper ohmic contact between silicon and aluminum. Finally, four devices were fabricated with and without tunnel layers and TiO_2 layers for photovoltaic application, as discussed in **Table 1**.

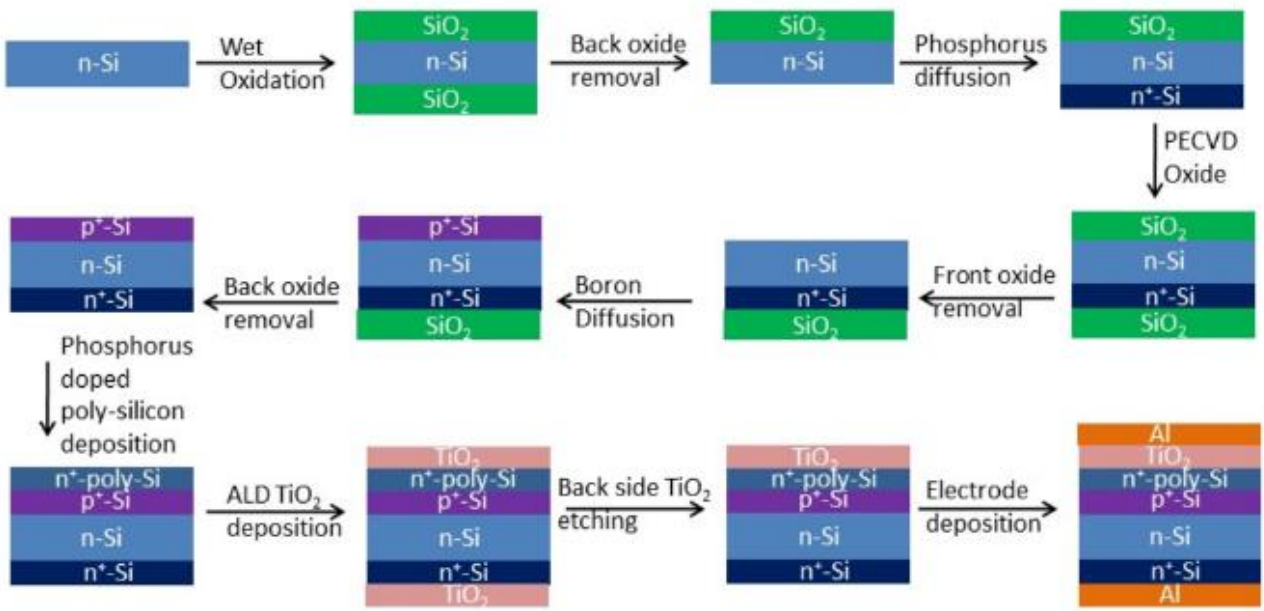

Fig. 2. Fabrication steps of the poly-silicon/c-silicon tunnel diode-based solar cells.

Table 1. Details of fabricated devices: A (without tunnel layer, homo-junction silicon cell only (n^+-Si/n-Si/p^+-Si)), B (silicon homo-junction solar cell with 195±10 nm thick tunnel layer), C (silicon homo-junction solar cell with 95±5 nm thick tunnel layer), and D (device C with 45±2 nm additional TiO_2 layer.

Device Label	Poly-silicon (nm)	TiO_2 thickness (nm)	Forming gas anneal
A (n^+-Si/n-Si/p^+-Si)	-	-	Yes
B(n^+-Si/n-Si/tunnel diode)	195±10	-	Yes
C(n^+-Si/n-Si/tunnel diode)	95±5	-	Yes
D(n^+-Si/n-Si/tunnel diode/TiO_2)	95±5	45±2	No

Characterization

Grazing-incidence X-ray diffraction (GIXRD) measurements were done in a Rigaku Smart Lab system using CuK_α (λ=1.54Å) X-ray source and 0.3° incident angle. Films were imaged using a Zeiss ULTRA55 scanning electron microscope. Current-voltage characteristics were measured using Agilent B1500A. Solar cell efficiency was measured using an Abet Class AAA solar simulator under a standard AM1.5G spectrum. The solar simulator was calibrated using a standard silicon solar cell. External quantum efficiency (EQE) was measured using a Bentham PVE300 system. Minority carrier recombination lifetime measurement was done by microwave detected photoconductivity decay, using MDP-Spot by Freiberg instruments. Minority carrier lifetime data was recorded at injection level (Δn) $7.2\times10^{16}cm^{-3}$ with a pulsed laser (λ=980 nm).

Results and discussion

Phosphorus doped poly-silicon film was deposited using LPCVD for 30 minutes. Scanning electron microscopy shows that the film was 195±10 nm thick (**Fig 3(A)**). The high-resolution top image (inset) reveal that film is smooth and continuous, too (**Fig. 3(A)**). The grazing incident X-ray diffraction (GIXRD) peaks can be indexed

to Si (111), (220), and (311) (**Fig. 3(B)**), showing that the films are polycrystalline [**15,16**]. Si (100) peak due to the substrate is not seen because of the small incident angle (0.3°). Using the Scherrer equation on (220) peaks full width at half maxima (FWHM), the average crystallite size is estimated to be ~21.5 nm [**17**]. The sheet resistance of the doped poly-silicon film was extracted from Hall measurements. The sheet resistance of 195±10 nm thick film is ~2.4×10^3 Ω/□, with a carrier concentration of ~10^{19} cm^{-3}.

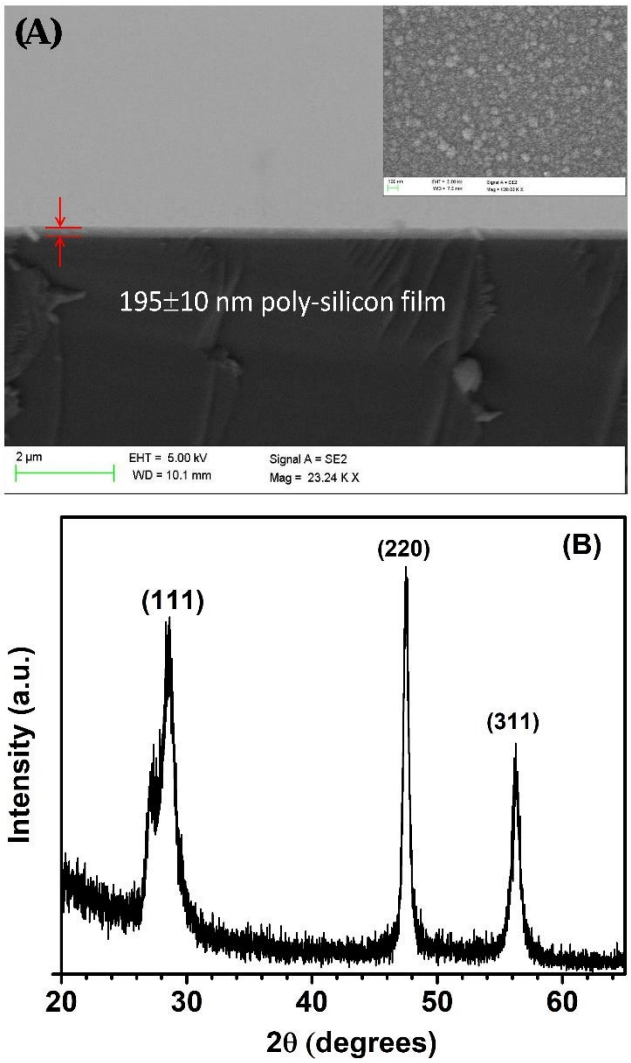

Fig. 3. (A) SEM images of a 195±10 nm thick poly-silicon film, (B) XRD pattern of poly-silicon film.

Fig. 4 shows the J-V characteristics of the control device without tunnel diode (just substrate, Al/p^{++}-Si/Al) and test structure with the n^{++} /p^{++} tunnel diode. Devices with the tunnel-diode can support higher currents, ~1 kA/cm^2 instead of 0.4 kA/cm^2 at 0.1 V. The series resistance due to the highly-doped wafer (~0.001 Ω-cm) is expected to be ~5×10^{-5} Ω.cm^2. Assuming the contribution of contact resistance in the two devices is similar, an upper-bound of the contact resistance is extracted, which is ~0.1 mΩ-cm^2. For a 20% efficient solar cell operating at a short circuit current density of 40 mA/cm^2, the Ohmic losses due to the tunnel diodes are 0.0008 % of the total output of the solar cell. Römer *et. al.*, earlier reported the contact resistance of 12 ± 7 mΩ-cm^2 for Al/ITO/poly-Si/SiO_x/c-Si test structure [**10**].

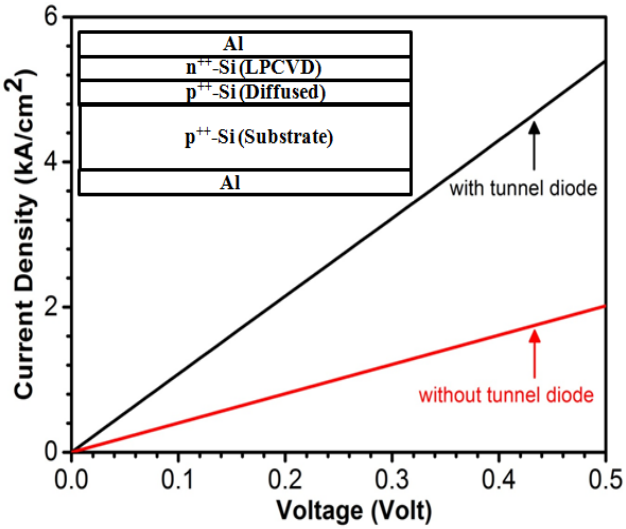

Fig. 4. J-V characteristics of the devices with and without tunnel diode (just substrate, Al/p^{++}-Si/Al).

Next, to observe the photovoltaic application of tunnel diode, four sets of devices were fabricated; details of each are given in Table1. Device A is a control device that is purely silicon homo-junction (n^+-Si/n-Si/p^+-Si, solar cell in absence of poly-silicon and TiO_2 layers). Emitter thickness in all the four devices is ~800 nm with doping concentration ~2×10^{20} cm^{-3}, while back surface field (BSF) thickness is ~740 nm with doping concentration ~2×10^{20} cm^{-3} [**18**]. Further, all the devices are planar, without any texturing and anti-reflection coating. The difference in device B and device C is only the thickness of the poly-silicon layers. While device D has an additional layer of TiO_2 (45±2 nm) than device C. The details of cross-sectional SEM and XRD patterns for the poly-silicon layer in Device B are already discussed in **Fig. 3(A)** & **Fig. 3(B).** The phosphorus doped poly-silicon films were deposited for 10 minutes in device C and device D (Table 1). The cross-sectional SEM image shown in **Fig. 5(A)**, confirms the 95±5 nm thickness of the poly-silicon film (for 10 minutes deposition). The measured carrier concentration in doped poly-silicon film is ~10^{19} cm^{-3}, using Hall measurement. The scanning electron microscopy further shows that the ALD TiO_2 film is 45±2 nm thick (**Fig. 5(B)**). The GIXRD pattern of TiO_2 (supplementary data S1) shows the film is polycrystalline, with peaks indexed to anatase TiO_2 (101), (004), (200), (105), and (204) [19-20]. Given the low deposition temperature, it is not surprising that the TiO_2 films are polycrystalline and anatase.

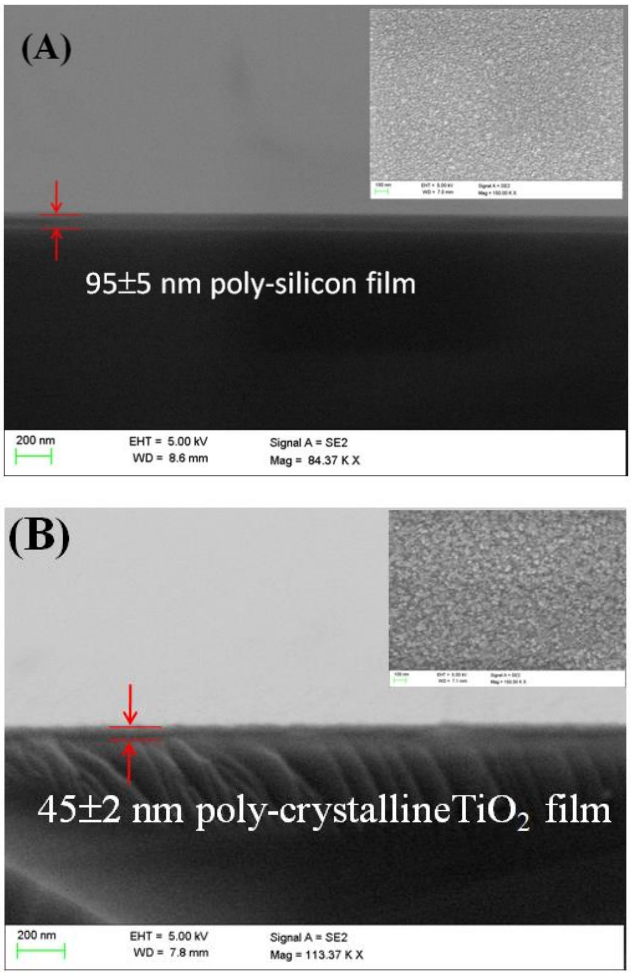

Fig. 5. Cross-sectional SEM images of (A) 95±5 nm thick poly-silicon film and (B) 45±2 nm thick polycrystalline TiO_2 film.

The J-V characteristics of all the devices show rectifying characteristics (**Fig. 6(A)**). Using the two-diode model, the diffusion (J_{01}) and space-charge recombination (J_{02}) saturation current densities can be extracted (**Table 2**). J_{02} is estimated below 0.4 V while J_{01} calculated around 0.5V corresponding to ideality factor 2 & 1 respectively [**18, 21-23**]. Diffusion saturation current in device A is nearly one order less than devices B, C & D. Poly-silicon tunnel layer is known to increase the surface recombination velocity, which explains the increase in J_{01}.

Space-charge recombination (J_{02}) is a direct function of the effective minority carrier recombination lifetime (τ_{eff}) [**22,24-25**]. The measured τ_{eff} for devices A, B, C, and D is 215.4 µs, 336.4 µs, 125.9 µs, and 144.3 µs, respectively (Supplementary data S2). The recombination lifetime of devices C and D is lower, arguably due to the higher surface recombination. The negative voltage region in J-V characteristics is related to the leakage current of the different devices [**26**]. The lower leakage current density in device A confirms its best shunt behavior than other devices. The shunt resistance of device B has a higher value than device C probably due to the higher thickness of poly-silicon.

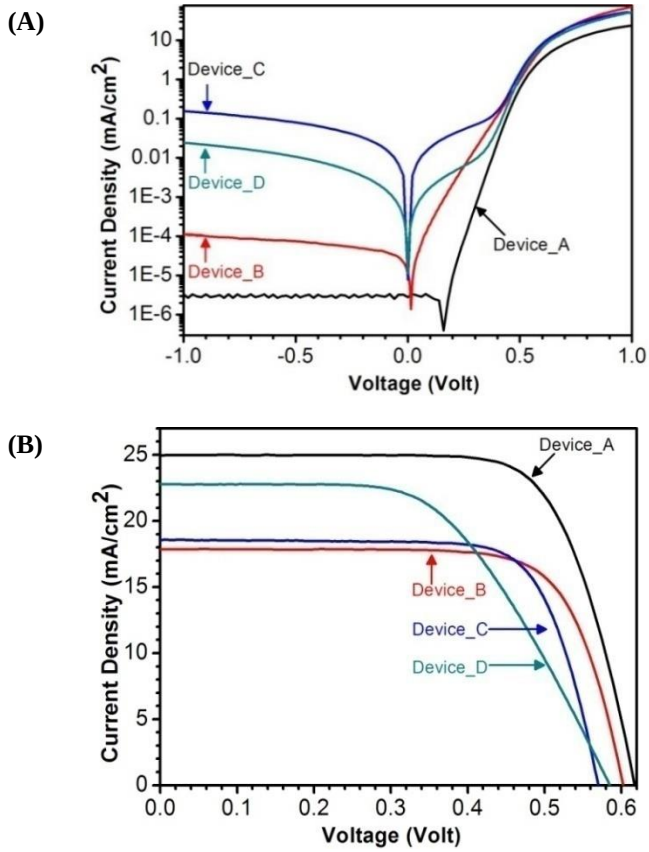

Fig. 6. J-V characteristics of as-fabricated solar cells: (A) in dark and (B) under AM 1.5G.

Table 2: Comparison of different solar cell performance parameters with and without tunnel layer.

Name	Device Details	J_{01} (nA/cm^2)	J_{02} (µA/cm^2)	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (%)	R_{Shunt} (kΩcm^{-2})	Rs (Ωcm^{-2})	η (%)
A	Planar	2.7	-	25.0	616	72.3	73.3	0.7	11.1
B	Planar +195±10 nm n-poly-Si	46	-	17.9	601	74.0	38.0	-	7.9
C	Planar + 95±5 nm n-poly-Si	90.1	13	19.7	580	73.0	2.5	1.1	8.3
D	Planar + 95±5 nm n-poly-Si +45±2 TiO_2	12.6	0.90	22.8	584	56.3	14	3.1	7.5

Under AM1.5G illumination, the device show typical solar cells characteristics (**Fig. 6(B)**). Device A ($Al/n^+/n/p^+/Al$) shows the current density of 25 mA/cm^2. This value is lower than state-of-art silicon devices, mostly due to the absence of texturing and anti-reflection coating (ARC). With a similar device architecture and 80 nm thick SiNx ARC, Mailoa *et. al.* reported a current density of 31.6 mA/cm^2 [**9**]. Sub-optimal emitter design and associated absorption losses may also contribute to the low Jsc. Here, the emitter doping is 2×10^{20} cm^{-3}, and the thickness is 0.80µm. The carrier diffusion length in 10^{20}cm^{-3} doped emitter is ~500 nm, limited by Auger recombination. So, there is a ~300 nm thick dead-layer at the top surface [**27**], which causes an estimated J_{SC} loss of 3 mA/cm^2. The presence of the dead region can also be inferred from the external quantum efficiency (**Fig. 7**), which clearly shows low absorption (<28%) below 440 nm.

The device B shows a J_{SC} that is 7.1 mA/cm^2 lower than device A. Part of this decrease can be blamed on absorption losses in the poly-silicon over layer. The 195±10 nm thick poly-silicon increases the effective dead layer to 495 nm, which causes a further loss of 3 mA/cm^2. External quantum efficiency (**Fig. 7**) also shows that the absorption loss occurs across the blue-green spectrum (<500 nm), which is consistent with a 495 nm thick dead region. The balance loss of 4 mA/cm^2 is probably due to recombination at the poly-silicon/silicon interface. Device C has a just 95 nm thick poly-silicon layer and hence lower absorption losses than device B. Reduction in the dead layer by 100 nm is expected to improve Jsc by 1.7 mA/cm^2, which matches extremely well with an actual increase of 1.8 mA/cm^2. Lower absorption losses in the thinner tunnel junction improve the absorption of the blue photons (**Fig. 7**). The variations in Jsc for the same batch devices are shown in **Fig. 8(A)**.

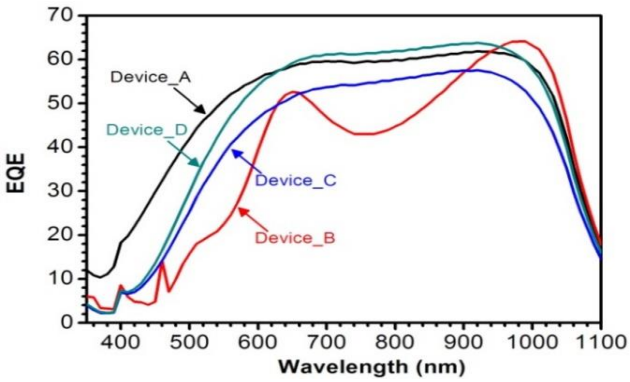

Fig. 7. External quantum efficiency spectra of silicon solar cells with and without tunnel layer as well as with an electron transport layer (TiO_2).

From Table 2, the open-circuit voltage for device A is 616 mV which is 15 mV more than device B. A higher value of V_{OC} in device A confirms a better collection probability than device B. This is further supported by the dark J-V characteristic, which validates the one-order less diffusion saturation current in device A than B. Surprisingly, device C has 20 mV less Voc than device B even though both devices (B & C) have similar process parameters except tunnel layer thickness. Interestingly, an additional space charge region recombination current (J_{02}) is also present in device C along with diffusion saturation current (J_{01}). Furthermore, the diffusion saturation current density in device C is nearly double of that device B (**Table 2**). Device D shows a similar trend to device C except for recombination saturation current which is nearly seven times less than device C. Mailoa *et al.*, reported ~600 mV open-circuit voltage with a 30 nm thin tunnel layer for a similar structure [**9**]. However, device B has 601 mV open-circuit voltage equivalents to the reported value with a 195 nm tunnel layer. While other devices' C & D open-circuit voltage is less than 600 mV which further needs optimization for improvement. The variations in Voc of same batch devices are shown in **Fig. 8(B)**.

The series resistance for devices A and C is ≤1.1 Ω-cm^2 which is very close (1.03 Ω-cm^2) to what was reported by Mailoa *et al.* for a similar structure [**9**]. The lower series resistance provides a higher fill factor, as shown in **Table 2**. In contrast, device D has higher series resistance (3.1 Ω-cm^2) than devices A and C. For devices A, B & C, forming gas annealing has been performed, while device D is untreated. The downside of the higher series resistance in device D is the lower FF (~56.3%). Ideally, the shunt resistance in planar silicon devices is ≥10^3 Ohm-cm^2, which is envisioned in **Table 2**. The variation in FF and efficiency of the same batch devices is discussed in **Fig. 8**. Overall, device D is showing 7.5% efficiency. Structures of devices B, C & D having tunnel diodes can be further used to fabricate the monolithic perovskite/silicon tandem solar cell (ETL/perovskite/TiO_2/n^+-poly-Si/p^+-c-Si/n-c-Si/n^+-c-Si) [**9, 27**]. Werner *et al.*, reported a similar structure using ZTO as a recombination layer [**28**]. While ITO as a recombination layer has been mentioned by Bush *et. al.*, with silicon heterojunction (SHJ) structure [**29**]. However, in this work the recipe needs further optimization for better performance.

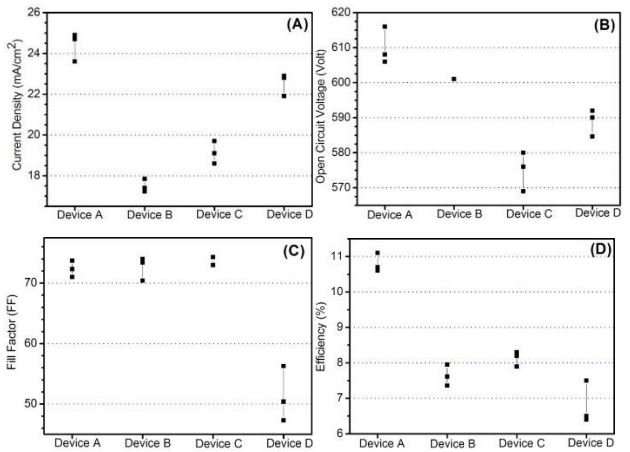

Fig. 8. Performance of various solar cells (3 cells in each group) in terms of (A) short circuit current density, (B) open-circuit voltage, (C) Fill-Factor, and (D) efficiency.

Conclusion

In conclusion, we successfully fabricated a doped poly-Si/c-Si tunnel diode. Hall measurements confirm the high doping (~10^{19} cm^{-3}) in poly-silicon, while the J-V characteristic demonstrates the current density ~10^3 A/cm^2 for tunnel diode test structure at 0.1 volts. The estimated contact resistance and efficiency loss for tunnel diode test structure is ~10^{-4} Ω-cm^2 and 0.0008%, respectively. The efficiency of stand-alone silicon cells in the absence of texturing and anti-reflection coating is 11.1 %. While, after integrating a doped poly-silicon layer (195±10 nm) over a stand-alone silicon cell, the efficiency becomes 7.9%. This efficiency further improves up to 8.3% by thinning down the poly-silicon layer to 95±5 nm. A thin poly-silicon layer improves the absorption of the blue photons and enhances the performance. A ~40 nm thick layer of TiO_2 has been mounted over a poly-Si/c-Si cell, which produces 7.5% efficiency and supports the device structure for tandem cell application. However, the recipe needs further optimization to improve the device's performance.

Acknowledgments

Author wish to acknowledge Centre for Nano Science and Engineering (CeNSE), IISc, Bangalore, for providing all the fabrication and characterization facilities during this work.

Keywords

Tunnel diode; poly-silicon; solar cell; recombination.

Supplementary Data Link

References

1. Green, M.; et. al.; Progress in Photovoltaics: Research and Applications, **2020**, *28(7)*, 629.
2. Richter, A.; Hermle, M.; Glunz, S.; *IEEE Journal of Photovoltaics*, **2013**, *3(4)*, 1184.
3. Swanson, R.; Proc. IEEE 31st Phtotvolt. Spec. Conf.; **2005**, 889.
4. Schäfer, S.; Brendel, R.; *IEEE Journal of Photovoltaics*, **2018**, *8 (4)*, 1156.
5. Ren, Z.; et. al.; *Solar Energy Materials and Solar Cells*, **2017**, *160*, 94.
6. Rolland, A.; Pedesseau, L.; Huang, Y.; Weng, S.; et. al.; Computational design of high-performance hybrid perovskite on silicon 2-T tandem solar cells based on a tunnel junction; international conference on numerical simulation of optoelectronic devices (NUSUD), Copenhagen, Denmark, July **2017**.
7. Rolland, A.; Pedesseau, L.; et. al.; *Optical and Quantum Electronics*, **2018**, *50*, 21.
8. Fave, A.; Lelièvre, J.F.; Gallet, T.; et. al.; *Energy Procedia*, **2017**, *124*, 577.
9. Mailoa, J.P.; et. al.; *Applied Physics Letters*, **2015**, *106(12)*, 121105.
10. Römer, U.; et. al.; *Solar Energy Materials and Solar Cells*, **2014**, *131*, 85.
11. Römer, U.; Ph.D. dissertation, Gottfried Wilhelm Leibniz Universität, Hannover; **2015**.
12. Peibst, R.; et. al.; *IEEE Journal of Photovoltaics*, **2019**, *9(1)*, 49.
13. Luderer, C.; et. al.; *APL*, **2019**, *115(18)*, 182105.
14. Pierson, H.O.; CVD Processes and Equipment, in Handbook of chemical vapor deposition: principles, technology and applications, 2nd ed., William Andrew Publishing, LLC Norwich, New York, USA, 1 (1999) 108.
15. Zhu, M.; et. al.; *Solar energy materials and solar cells*, **2000**, *62*, 109.
16. Lee, J.C.; et. al.; *Solar energy materials and solar cells*, **2002**, *74*, 233.
17. Dalchiele, E.A.; et. al.; *Solar energy materials and solar cells*, **2001**, *70(3)*, 245.
18. Singh, V.K.; Nagaraju, J.; Avasthi, S.; *Current Applied Physics*, **2019**, *19(3)*, 341.
19. Wang, Y.; et. al.; *Solar Energy Materials and Solar Cells*, **2017**, *161*, 297.
20. Attar, A.S., Hassani, Z.; *Journal of Materials Science & Technology*, **2015**, *31(8)*, 828.
21. Pierret, R.F.; Semiconductor Device Fundamentals; 2nd Ed.; Dorling Kindersley Pvt. Ltd.; India, **2008**, pp. 235-300.
22. Alam, M. A.; ECE606: Principles of Semiconductor Devices; Department of Electrical Engineering, Purdue University, Nov., **2008**.
23. Singh, V.K.; Nagaraju, J.; *Adv. Mater. Lett*, **2015**, *6(7)*, 600.
24. Aberle, A.G.; Crystalline silicon solar cells: advanced surface passivation and analysis; 2nd Ed.; Centre for Photovoltaic Engineering. University of New South Wales; **1999**, pp. 13-46.
25. Ravindra P.; Mukherjee, R.; Avasthi, S.; *IEEE Journal of Photovoltaics*, **2017**, *7(5)*, 1278.
26. Yang, D.; et. al.; *Nano Energy*, **2021**, *84*, 105934.
27. Honsberg, C., Bowden, S.; http://pveducation.org/pvcdrom/design/material-thickness, Solar Power Lab, Arizona State University, USA,
28. Werner, J.; et. al.; *Applied Physics Letters*, **2016**, *109(23)*, 233902.
29. Bush, K.A.; Palmstrom, A. F.; et. al.; *Nature Energy*, **2017**, *2(4)*, 1.