Growth and characterization of graphite doped CdTe/CdS thin film heterojunction

Muhammad Asghar[1*], Ya Hong Xie[2], M. Asif Nawaz[1], Hammad M. Arbi[1], M. Y. Shahid[1], F. Iqbal[1], Waqas Khalid[1]

[1]*Department of Physics, The Islamia University of Bahawalpur, 63100, Pakistan*
[2]*Department of Applied Materials & Engineering, UCLA, USA*

*Corresponding author. Tel: (+92) 3017724897; E-mail: mhashmi@iub.edu.pk

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Abstract

Doping is a notable factor to improve the performance of CdTe/CdS heterojunction solar cell. Graphite doped CdTe/CdS heterojunction on Si (1 1 1) substrate has systematically fabricated by thermal evaporator method under medium vacuum (10^{-4} torr) condition. Characterization of doped CdTe/CdS film was carried out by various diagnostic techniques such as X-ray diffraction (XRD) exhibits the polycrystalline structure of cubic phase CdTe and hexagonal phase CdS, scanning electron microscopy (SEM) shows the smoothening of the film, energy dispersive X-ray (EDX) confirm the elemental composition found in the film and current-voltage (I-V) analysis suggests the diode like properties where the current is slightly increased by the doping of graphite into CdTe/CdS heterojunction compared to the reported literature. Analysis of I-V characteristics has been made to investigate the current conduction mechanism in CdTe/CdS heterojunction.

Keywords: CdTe, CdS, graphite, heterojunction.

Introduction

Semiconductors are the foundation of modern electronics because of the ability to change their conductivity by introducing impurities in their lattice structure. The viability of solar energy as a preferably source of energy depends on developing low-cost, large-area manufacturing processes. These would certainly take place by adopting cells based on a thin film device. Of many choices, CdS/CdTe heterojunctions have proved probably the most attractive and promising structure for possible photovoltaic application **[1]**. Effective improvement of the device structure is only possible based on a complete understanding of the device properties. Those properties are determined by structural influences as well as by the electronic structure of the different interfaces **[2]**. If both the p-type and the n-type regions are of the same semiconductor material, the junction is called a homojunction. If the junction layers are made of different semiconductor materials, it is a heterojunction. A heterojunction is created when two different layers of crystalline semiconductors are placed in conjunction or layered together with alternating or dissimilar band gaps. Mostly utilized in-solid-state-electrical devices, heterojunctions can also be formed between two semiconductors with different properties such as one that is crystalline while the other is metallic. When the function of an electrical device or device application depends on more than one heterojunction, they are placed in formation to create what is called a heterostructure. As deposited CdS is n-type and has wide bandgap ~ 2.4 eV making it suitable as a window layer and CdTe has a band gap of ~ 1.5 eV making it suitable as absorber layer. CdTe has long been a leading material in thin film solar cell fabrication. The polycrystalline layers of a CdS/CdTe cell can be deposited using a variety of low cost techniques, such as close-spaced-sublimation (CSS), physical vapor deposition (PVD), chemical bath deposition (CBD), magnetron sputtering **[3]** and etc. Thin film solar cells are still having a serious development problem, considering that the efficiency increase progresses are barely being noticed. Technological variations resulting in structural modifications of thin films and changes in physical processes might lead to progresses. The quality of thin semiconductor films and devices based on them is highly influenced by the deposition technology **[4].** A number of reports are available on the characterization of CdTe/CdS heterojunction devices **[2, 5-7].** The CdS/CdTe interface is believed to be a limiting factor for solar cell. Nearly all of the recent solar cells are based on heterojunctions **[3, 8-14]**, hence it is very necessary to study, understand and fabricate heterojunctions as a first step towards making better solar cells.

The present work goal is to make thin film of graphite doped CdTe/CdS heterojunction. Silicon (1 1 1) is used as

a substrate due to the mechanical robustness and the high thermal conductivity which can mitigate the degradation of cell-performance from the heating during light concentration [**15**]. To the best of our knowledge, no study has been published that investigates the effect of graphite doping on CdTe/CdS heterojunction. We have doped graphite into our heterojunction to investigate the changes that might occur in the structural and electrical properties of the heterojunction. In the following, experimental, results and discussion and conclusion are described.

Experimental

The requirements of CdTe/CdS thin film heterojunction are simple in comparison to most routinely produce electronic and optoelectronic structures, it comprises:

(i) a back metal Ohmic contact

(ii) a p-CdTe absorber layer

(iii) an n-CdS window layer

(iv) a front Ohmic contact

The materials used in this experiment were Si (1 1 1) substrate, Cu source, CdTe source, CdS source, graphite source and indium source. Before deposition CdTe/CdS heterojunction, Si wafer was cleaned with acetone, isopropyl alcohol and deionized water with ultrasonic cleaner for 30 minutes, then dipped for 10 minutes into hydrofluoric acid to remove the oxide layer. The substrate was loaded into the thermal evaporator unit and after achieving vacuum of 5 x 10^{-4} Pa, the Cu was evaporated on to the Si substrate first and a good Cu thin film was obtained. After giving ample time for Cu thin-film to settle down to the room temperature, the crush diffused graphite doped CdTe pellet was evaporated on to ~2/3rd area of Cu thin film substrate (as Cu intended to serve as back contact for heterojunction and saved ~1/3rd area of Cu film to use as a back contact). After that, the graphite doped CdS was evaporated onto the CdTe surface. Now for the front contact, indium was chosen as it is the best suited candidate according to the reported literature [**16**]. Indium was evaporated and small round-shape front contacts of indium were fabricated onto the heterojunction by the help of a porous ceramic to cover the sample.

The samples were grown by using DM-700C vacuum coating system by Beijing Beiyi. For studying the morphological, structural and electrical properties, SEM, EDX, XRD and I-V characterizations were performed. SEM images and EDX results were taken by Jeol JSM 6600LV equipped with elemental analyzer unit. Structural properties were characterized with a Phillips PW3710 XRD. Current–voltage measurements were performed under simulated standard testing conditions (AM1.5 G, 1000 W/cm^2, and cell temperature 25 ℃) by HP 4140 LCR meter.

Results and discussion

As seen in **Fig. 1 (a),** the typical schematic diagram of a CdTe/CdS heterojunction cell is composed of 4 layers:

1. An ohmic contact which is called front contact (made by indium-metal in circular shaped).
2. A CdS film which is so called window layer made on the top of CdTe layer.
3. A CdTe film which is absorber layer
4. The film of copper made on Si-substrate which is called back contact.

The as-grown graphite doped CdTe/CdS heterojunction sample is shown in **Fig. 1 (b).** The indium front contacts in the form of small dots and a copper thin film strip of back contact can be seen. The area of the substrate was ~ 0.564 cm^2.

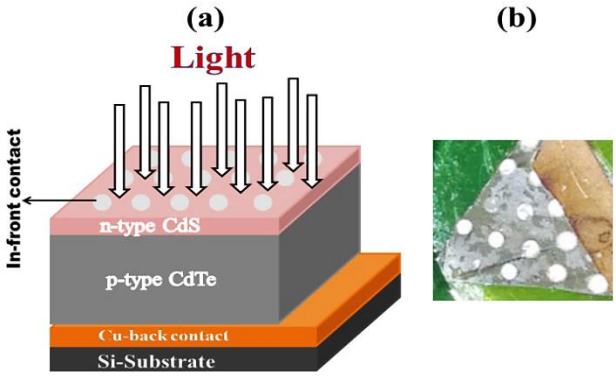

Fig. 1. (a) A typical schematic diagram of CdTe/CdS heterojunction (b) As grown graphite doped CdTe/CdS heterojunction with indium front contacts and Cu back.

X-ray diffraction spectroscopy

Fig. 2 shows the XRD spectra of the as-deposited graphite doped CdTe/CdS thin films using Cu Kα radiation having wavelength 1.5414 Å to evaluate the crystallographic properties of the thin films. The results indicate that the films have polycrystalline structure of CdTe cubic phase and CdS hexagonal phase.

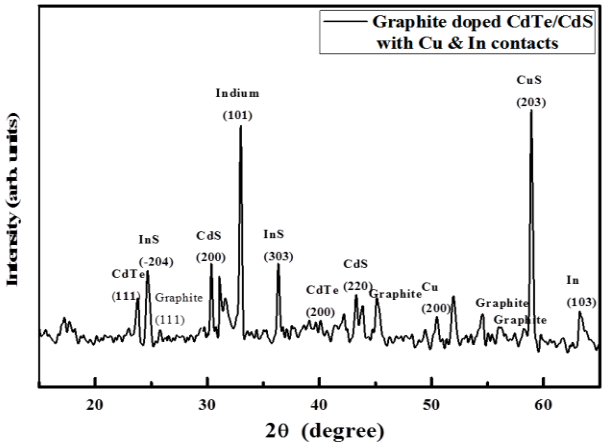

Fig. 2. XRD Spectra of the graphite doped CdTe/CdS heterojunction.

The spectra show different peaks at different angles having 2Θ equal to for CdTe at 23.7˚ and 39.3˚, for CdS at 30.6˚ and 43.8˚, for Cu at 50.4˚ and for In at 32.9˚ and 63.2˚. These peaks have miller indices, for CdTe (111) and (2 0 0), for CdS (2 0 0) and (2 2 0), for Cu (2 0 0), for In (1 0 1) respectively and for graphite at 45.1˚, 54.5˚, 55.9˚. Other than these peaks, the peak for InS at 24.5˚ and for CuS at 58.6˚ are also evident. The assigned peaks of all the elements are confirmed from their respective JCPDS cards. The major peaks are not reasonably shifted by the graphite addition as compared to reported literature **[4, 6, 17, 18]**.

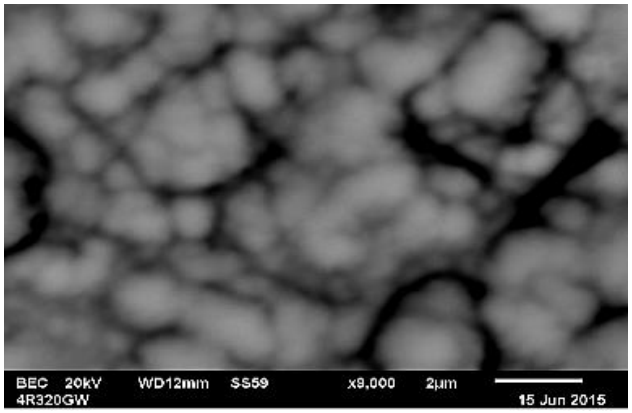

Fig. 3. SEM image of the surface of graphite doped CdTe/CdS heterojunction.

Scanning electron microscopy

SEM micrograph of as grown graphite doped CdTe/CdS heterojunction shows in **Fig. 3** which reveals the grown heterojunction thin film covers the substrate completely although the surface is not so much smooth. The ups and downs formed onto the surface of thin film can be seen. No major pinholes are seen for these dense samples and the substrate surface area is completely covered. In this regard, the results suggest that the grown film may have formed a heterojunction as confirmed by I-V measurements. The **Fig. 2** shows the surface morphology of as grown film.

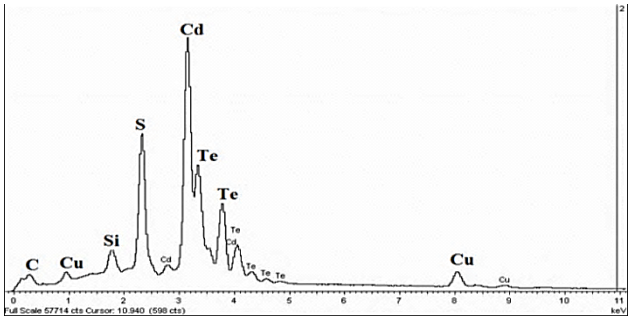

Fig. 4. EDX graph of graphite doped CdTe/CdS heterojunction.

Energy dispersive x-rays spectroscopy

The EDX graph is shown in **Fig. 4**. The results reveal cadmium, tellurium and sulphur as major components while copper and graphite as minor components of the graph.

Current-voltage measurements

The Current-Voltage (I-V) measurements of the as grown heterojunction are shown in the **Fig. 5**. The I-V measurements were taken in the dark and under the light respectively. For the dark I-V measurements, the grown graphite doped CdTe/CdS heterojunctions was placed in a small closed black box that was connected with LCR meter to record I-V measurements. The recorded data is plotted in **Fig. 5**. For measurements in the light, the heterojunction was placed under simulated standard testing conditions (AM1.5 G, 1000 W/cm^2, cell temperature 25 ˚C) and with the help of LCR meter the I-V readings were recorded as shown in **Fig. 5**. It is clearly seen from figure that in the present of light the value of conduction current is large as compared to the dark.

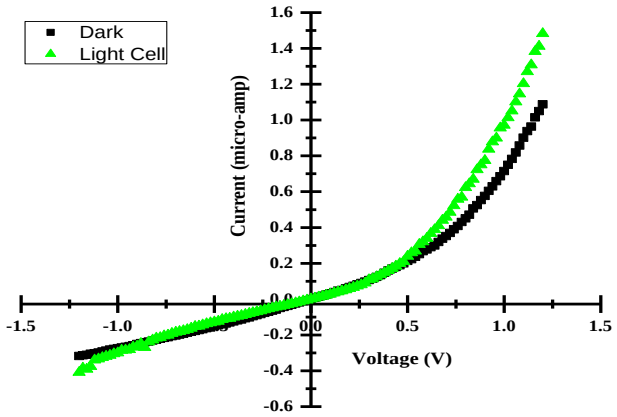

Fig. 5. I-V measurements of as grown graphite doped CdTe/CdS heterojunction.

A detailed analysis of I-V characteristics has been made to establish the current flow mechanism. Recombination at interface is the possible way of conduction where current can be described by the following equation

$$I = I_S \exp\left(\frac{qV}{nkT}\right)\left\{1-\exp\left(\frac{-qV}{kT}\right)\right\} \quad (1)$$

where, I_S is the reverse saturation current, k is Boltzmann constant, q is the electronic charge, T is the absolute temperature and n is the ideality factor.

Fig. 6 (a) show the plot of ln(I/(1-exp(-qV/kT))) Vs. V at low voltage which indicate that the current is dominated by recombination at the interface. Recombination is the process where an electron moves from the conduction band to the valence band so that a mobile electron–hole pair disappeared. Normally volume impurities and surface imperfections are the sites of recombination. The recombination component of the current is likely to be more important in high barriers, in material of low life time, at low temperatures and at low forward voltages [**19**]. **Fig. 6 (a)** clearly shows the two distinct regions of conduction, having different values of n. At low voltage (Region I: V < 0.4V) the value of n is

2.62 whereas at higher voltage (Region II: > 0.4V) the value of n is 4.16. It has been reported that recombination of carriers at the interface due to the defects produced by lattice mismatch and ohmic losses lead to higher ideality factor **[20, 21].** For higher voltages, Eq. (1) can be approximated as

$$I=I_S \exp\left(\frac{qV}{nkT}\right) \quad (2)$$

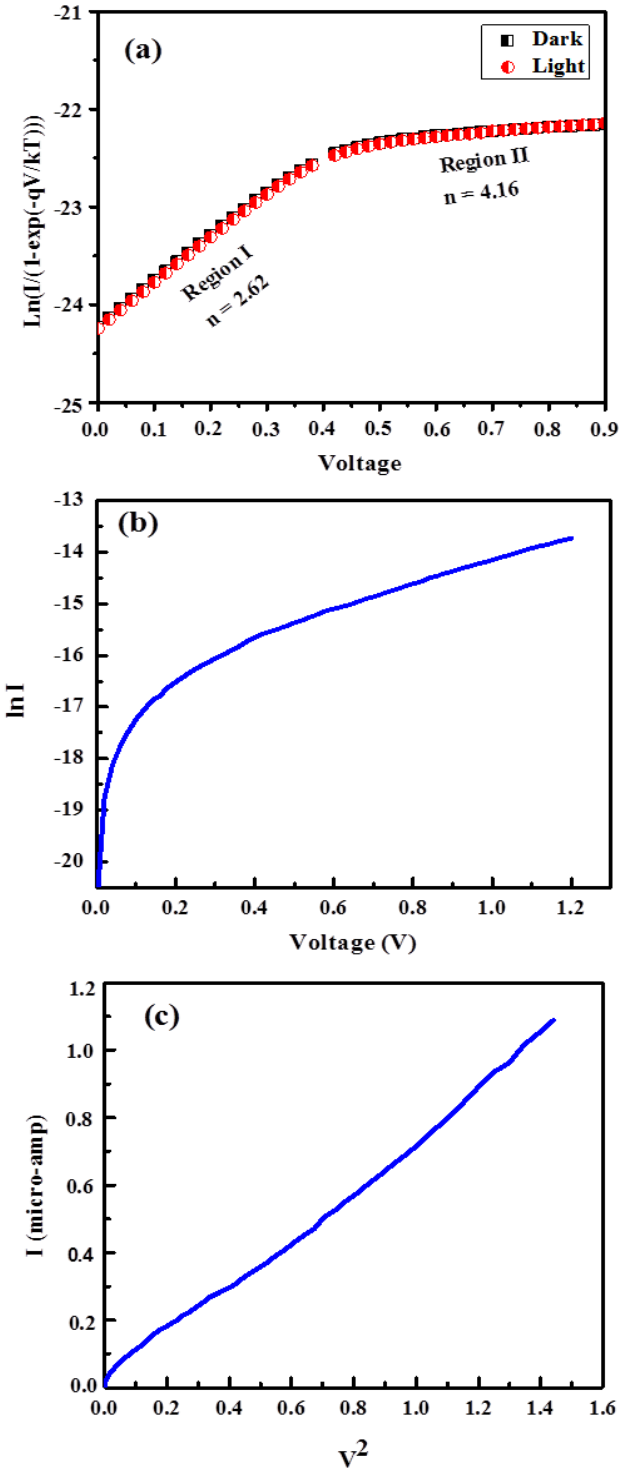

Fig. 6. (a) ln(I/1-exp(-qV/kT)) vs. V at low voltage (b) ln I vs. V (c) I vs. V^2 of the as grown graphite doped CdTe/CdS heterojunction.

The plot of ln I vs. V for the heterojunction is shown in **Fig. 6 (b)**. Non-linearity in the plot at higher voltage region rules out the current conduction by recombination mechanism in this region [**22**]. At higher voltages, current varies as square of the voltage as given in **Fig. 6 (c).** This suggests that, in this region, current is controlled by space charge limited conduction (SCLC) and allows us to use space charge limited (SCL) theory for I-V analysis.
In the SCLC region, current can be related to the voltage as follows [**23**],

$$I=\frac{\varepsilon_r Nc}{8L^3 N_t} A\mu\varepsilon V^2 \exp\left(\frac{E_t}{kT}\right) \quad (3)$$

where, ε_r is the relative permittivity, Nc is the effective density of states, N_t is the concentration of traps with activation energy E_t, L is the film thickness, A is the device area, m is the mobility and **ε** is the permittivity. This mode of conduction can have a pronounced effect on the electrical properties of semiconductors at room temperature and below, because they normally have a low density of free carriers and charge unbalance can be easily produced by an applied voltage. The character and magnitude of SCL effects are determined largely by the presence of localized states which can trap and store charge in equilibrium with the free charge. Single carrier injected currents are necessarily space-charge limited and in a perfect trap-free insulator where all the injected carriers remain free and all contribute to the space-charge, the current flow is exactly analogous to that in a vacuum diode. The presence of traps generally reduces the current by capturing most of the injected carriers. As the injection level (applied voltage) is raised all the traps will eventually become filled and the current will rise sharply back to the trap-free value.

From the **Table 1**, we see slight increase in the current of current study as compared to undoped CdTe/CdS heterojunction results. The comparison of our measurements taken in dark vs. in light values is shown in **Fig. 5**. The data comparison reveals that the graphite doped CdTe/CdS heterojunction diode is better than previously reported heterojunction's performance as shown in **Table 2 [22, 24].**

Table 1. Lists the values of 2Θ and indexed hkl from the XRD spectra.

Element	2Θ (degrees)	Index hkl
CdTe	23.7˚ and 39.3˚	1 1 1 and 2 0 0
CdS	30.6˚ and 43.8˚	2 0 0 and 2 2 0
Cu	50.4˚	2 0 0
In	32.9˚	1 0 1
Graphite	26˚	1 1 1

Table 2. Comparison of I (micro-amp) vs. Voltage (V) for this study and reported literature.

	I (micro-amp) at 0.0 Volts	I (micro-amp) at 0.5 Volts	I (micro-amp) at 1.0 Volts	I (micro-amp) at 1.2 Volts
Mahesha et al. [21]	~0	~0.2	~0.30	~0.35
This study	~0	0.213	0.715	1.08

Conclusion

By using thermal evaporation technique, we have grown graphite doped CdTe/CdS thin-film heterojunction. The XRD revealed CdTe, CdS, Graphite and their compound's peaks dominating in the XRD spectra. The SEM result reveals the uniformly distributed but not so smooth surface of the as grown films. The EDX analysis revealed Cd, Te, S, C (Graphite), Cu and In as major components of the grown films. The I-V measurement proved the heterojunction's diode-like properties of the as grown graphite doped CdTe/CdS thin films and slight increase in the current amounts as compared to the reported literature. Recombination at interface dominates the current conduction at lower voltages whereas space charge limited conduction controls the current conduction at higher voltages. In principle, a good p-n heterojunction is successfully formed which is the main goal for this study.

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