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Impact of oxygen diffusion on the performance of HfO_2/GaAs metal-oxide-semiconductor field-effect-transistors

Anindita Das[1], Sanatan Chattopadhyay[1, 2*], Goutam Kumar Dalapati[3]

[1]*Centre for Research in Nanoscience and Nanotechnology (CRNN), University of Calcutta, JD2 Sector-III, Saltlake, Kolkata 700098, India*
[2]*Department of Electronic Science, 92 APC Road, University of Calcutta, Kolkata 700009, India*
[3]*Institute of Materials Research and Engineering, A*STAR, (Agency for Science, Technology and Research), 3 Research Link, Singapore 117602, Singapore*

[*]Corresponding author. E-mail: scelc@caluniv.ac.in

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ABSTRACT

In the current work, electrical performance of n-channel GaAs MOSFETs with HfO_2 gate dielectrics has been investigated by considering the impact of oxygen diffusion from gate dielectric layer. Initially, the HfO_2/GaAs MOS capacitors are fabricated and its relevant process recipe has been simulated. The key parameters are extracted from both the experimental and simulated results to calibrate the simulator. The extracted parameters are subsequently fed into the simulator to investigate electrical performance of n-channel GaAs MOSFETs with varying gate lengths. The elemental diffusion of oxygen at HfO_2/GaAs interface has also been incorporated since oxygen naturally diffuses into the GaAs layer during deposition and annealing steps and thereby alters the effective doping concentration in the channel. The diffused oxygen has been observed to improve electrical performance parameters such as transconductance and threshold voltage, however, degrades DIBL of the HfO_2/GaAs MOSFET devices. Copyright © 2016 VBRI Press.

Keywords: GaAs; HfO_2; MOSFET; threshold voltage; transconductance.

Introduction

The Si-based complementary-metal-oxide-semiconductor (CMOS) has been the workhorse of microelectronics where successive down scaling of the technology nodes has been the preferred route for sustained performance improvement. The excellent material properties of Si, SiO_2 and the reliability of SiO_2/Si interface have played a vital role for such four decades of progress [**1**]. However, such conventional scaling approach has been seriously challenged by the physics of materials and devices. The fundamental limit emerges from the aggressively scaled down ultrathin SiO_2 layer where several leakage current components due to quantum-mechanical tunneling becomes unexpectedly high. Also, the state-of-the-art interconnect delay has been almost 2-order of magnitude higher than the gate delay. Consequently, it has been difficult to meet different design challenges and data communication has been identified as one of the major challenges in the progress of silicon based computation [**2**]. To meet such requirement, on-chip optical interconnect is emerging as a potential substitute of electrical interconnect [**3-6**]. Effort is being devoted to develop all-Si optical integrated circuits combining both the advantages of Si-CMOS technology and optical interconnects. However, no remarkable breakthrough has been achieved so far due to the non-availability of suitable optical source from Si. A hybrid combination of Si-based CMOS technology and group III-V based optical source and detectors may be a solution. However, the integration of these two technologies is a real challenge and costly. In this regard, developing the gallium-arsenide (GaAs) based MOSFETs may be more advantageous over Si since it can meet both the requirements. The electron mobility of GaAs is ~ 6× higher than Si and therefore suitable for developing high-speed switching devices [**7**]. Also, the GaAs based technology is well matured for developing optoelectronic devices.

The benefits of developing GaAs-based MOSFETs are well known [**1**, **8-15**]. However, the main obstacle to fabricate GaAs-based MOSFETs is the lack of availability of high-quality gate insulators on GaAs substrates to meet the requirement for high performance switching devices. The main challenge is to reduce the mid-gap density of interface states [**1**]. Several reports are available where attempts have been made to grow SiO_2 as the gate insulator on GaAs substrate; however, these were not successful due to the lack of reliability of such insulators and the generation of an unacceptable level of interface states [**16-19**]. The main difficulty in growing oxides directly on GaAs substrate is the formation of Ga_2O_3 and As_2O_3 at the expense of surface Ga and As. The oxidation rate of Ga and

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As is different and it leads to the creation of a significantly high density of defects and interface states. Further, the diffusion of oxygen from the gate insulator layer towards GaAs substrate in a HfO_2/GaAs system becomes significant during HfO_2 deposition and subsequent process thermal cycles, leading to the generation of deep traps in its bandgap region and altering the effective channel doping concentration [**20-24**]. Consequently, the device characteristics as well as its performance parameters change significantly due to such oxygen diffusion.

The progress of atomic layer deposition (ALD) technique provides a unique opportunity to integrate high-quality gate dielectrics on GaAs [**25-28**]. Due to continuous effort to develop surface passivation techniques, it has been possible to create a high-quality interface with low defect density on GaAs. However, the reduction of hysteresis voltage for ALD high-k/GaAs gate stack is still challenging [**25, 27, 29**]. Recently, it has been shown that the development and implementation of an appropriate surface passivation step can improve interfacial quality and an interface state density as good as 6×10^{11} $eV^{-1}cm^{-2}$ has been reported [**30**]. Also, an attempt is made to fabricate surface channel MOSFETs on epi-GaAs for achieving good interfacial quality between the oxide and GaAs [**31**].

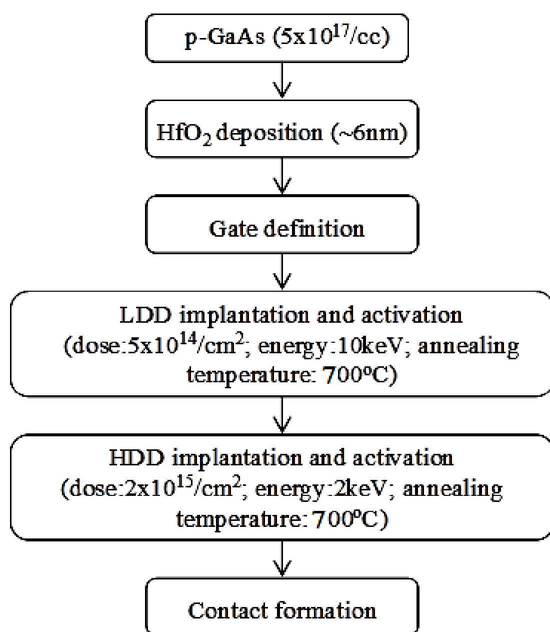

Fig. 1. Process steps simulated for fabricating the GaAs channel MOSFETs with HfO_2 gate insulator.

In the current work, the impact of oxygen diffusion from HfO_2 gate dielectric layer on the performance of GaAs channel MOSFETs has been studied. Initially, a process recipe for the fabrication of HfO_2/GaAs MOS capacitors has been simulated. Following the similar process flow such MOS capacitors are fabricated and characterized. The device parameters such as flat band voltage (V_{FB}), oxide thickness (t_{ox}), interface state density (D_{it}), fixed oxide charge (Q_F), and doping concentration (N_A) are extracted from the experimental measurements and fed into device simulator for the design of state-of-the-art HfO_2/GaAs MOSFETs. A process recipe for the fabrication of GaAs based MOSFETs by following a conventional approach has been developed and its electrical performance is obtained by simulating the structure with input data obtained from the experimental MOS capacitors.

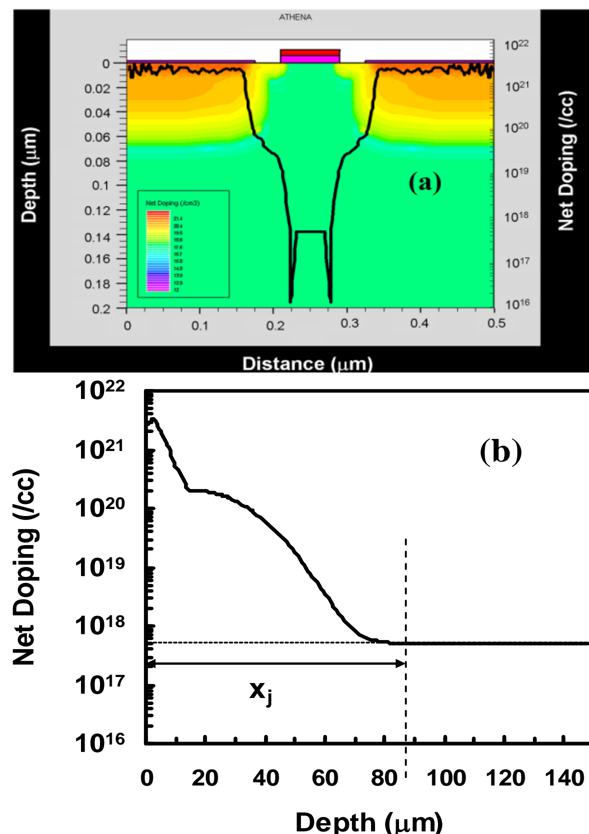

Fig. 2. (a) Simulated structure of an enhancement-mode n-channel HfO_2 / GaAs MOSFET along with doping profile of the MOSFET from source to drain end; (b) doping profile of the MOSFET along the depth of the channel to substrate.

Design and Simulation of HfO_2/GaAs MOSFETs

Details of the fabrication of HfO_2/GaAs MOS capacitors are described elsewhere [**32**]. The HfO_2/GaAs MOSFETs considered in the current work have been fabricated by simulating the process recipe as has been described in **Fig. 1**.

Fig. 2(**a**) shows the simulated structure of n-channel enhancement mode GaAs MOSFET with 6 nm HfO_2 gate dielectric layer, fabricated by using the process simulator ATHENA, available in SILVACO [**33**]. Also, the doping profile of the device along the channel from source to drain at a depth of 5 nm from the HfO_2/GaAs interface is overlaid. The nature of doping profile is appropriate for MOSFET operation since such doping controls the magnitude and nature of the longitudinal as well as transverse electric fields, thereby controlling its operation. The S/D doping concentration is obtained to be 2×10^{21} cm^{-3} whereas for the channel region it is obtained to be 5×10^{17} cm^{-3}. The maximum junction depth (x_j) is obtained to be ~87 nm from the plot of doping profile as shown in **Fig. 2**(**b**).

For simulating electrical characteristics of the device using ATLAS, the mobility degradation due to surface

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scattering at HfO_2/GaAs interface has been considered. The Lombardi inversion layer model has been incorporated through surface roughness mobility component, μ_{sr}, given by [**33**]:

$$\mu_{sr,n} = \frac{\text{DELN.CVT}}{\text{KN.CVT}} \tag{1}$$

where, the values for DELN.CVT and KN.CVT parameters are considered to be 5.82×10^{14} V/s and 2 respectively for GaAs for the current work [**33**]. The field-dependent mobility has been considered to provide a smooth transition of the carrier transport from low-field to high-field, following Caughey and Thomas expression, given by [**33**],

$$\mu_n(E) = \mu_{n0}\left[\frac{1}{1+(\frac{\mu_{n0}E}{v_{satn}})^{\beta_n}}\right]^{\frac{1}{\beta_n}} \tag{2}$$

where, E is the longitudinal electric field and μ_{n0} is the low-field electron mobility, v_{satn} is its saturation velocity.

Phonon transitions occur in presence of traps (or defects) within the forbidden gap of the semiconductor. This is essentially a two-step process and is included into the device simulator through Shockley-Read-Hall (SRH) recombination theory [**33**]:

$$R_{SRH} = \frac{pn - n_{ie}^{2}}{\tau_{p0}[n + n_{ie}\exp(\frac{E_T}{kT_L})] + \tau_{n0}[p + n_{ie}\exp(\frac{E_T}{kT_L})]} \tag{3}$$

where, E_T is the energy difference of the traps and intrinsic Fermi level, T_L is the lattice temperature in absolute scale and τ_{n0} and τ_{p0} are the electron and hole lifetimes, respectively.

As gate length of the MOSFET in the current work is considered to be scaled down to 20 nm, the quantum size effects are also included. The quantum size effects are modeled by solving the Schrodinger-Poisson's coupled equation along with the fundamental device equations. The solution of Schrodinger's Equation gives a quantized description of the density of states in presence of quantum mechanical confining potential variations. The calculation of the quantized density of states relies upon the solution of Schrodinger's equation [**33**].

$$-\frac{\hbar}{2}\frac{\partial}{\partial x}[\frac{1}{m_l}\frac{\partial \psi_{il}}{\partial x}] + E_C(x)\psi_{il} = E_{il}(x)\psi_{il} \tag{4a}$$

$$-\frac{\hbar}{2}\frac{\partial}{\partial x}[\frac{1}{m_l}\frac{\partial \psi_{it}}{\partial x}] + E_C(x)\psi_{it} = E_{it}(x)\psi_{it} \tag{4b}$$

where, E_{it} is the ith bound state energy for transverse mass, E_{il} is longitudinal, Ψ_{it} is the transverse wavefunction, Ψ_{il} is the longitudinal wavefunction, and E_C is the band edge energy.

In order to study the effect of oxygen diffusion on the device performance characteristics, DIFFUSION model has been introduced and the amount of oxygen diffusion for different thermal cycles has been studied. The diffusion process can be expressed as [**33**]:

$$\partial_n C_1 + K_S(C_1 - C_1^{*}) = G_1 \tag{5}$$

where, $\partial_n C_I$ is the projection of the interstitial flux vector on an inward pointing unit vector normal to the boundary, K_S is the effective surface recombination rate for interstitials, G_I is the generation rate at the interface of interstitials during annealing in an oxidizing ambient, and C_1^{*} is the equilibrium interstitial concentration.

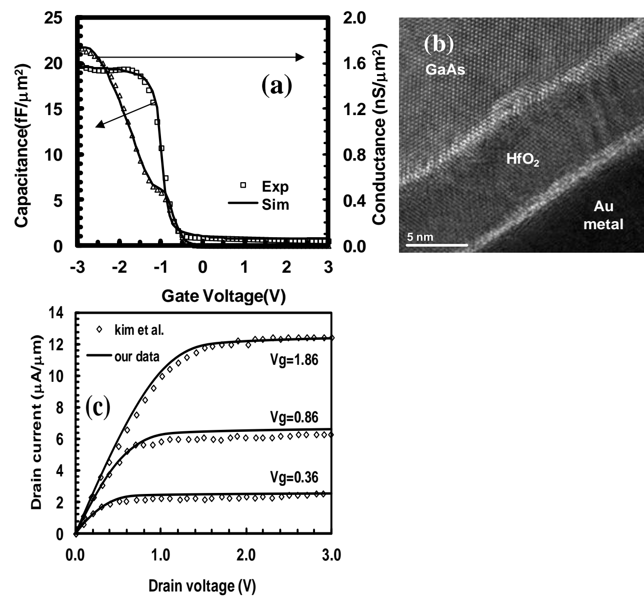

Fig. 3. (a) Experimental and simulated C-V and G-V characteristics of p-GaAs MOS capacitor with 6nm HfO_2 gate dielectric. (b) Cross-sectional HRTEM image of Au/ALD HfO_2/ GaAs stack with scale bar of 5nm. (c) Experimental and simulated I_D-V_D characteristics as a function of gate bias from depletion-mode MOSFET with L_g of 8 μm.

Table 1. Summary of the parameters used in the simulation.

Parameters	Values
Substrate doping	5×10^{17}cm^{-3}
S/D doping	2×10^{21}cm^{-3}
HfO_2 layer thickness [32]	6nm
Dielectric constant of HfO_2 layer [32]	25
Interfacial trap density at mid-gap [32]	~10^{11}cm^{-2}eV^{-1}
Fixed oxide charge [32]	~10^{12} cm^{-2}

Results and discussion

The MOS capacitors with similar specifications and material stacks have been fabricated following a standard process flow [**32**] and its electrical results are simulated and compared with experimental data. The plots of both experimental and simulated results are shown in **Fig. 3**(**a**) and the parameters used in the simulation are summarized in **Table 1**. It is apparent that the simulated results agree well with the experimental data, indicating the accuracy of the simulator as well as the models used. Thickness of the

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dielectric layer was measured from the transmission electron microscopy (TEM) image of ALD HfO_2 on bulk-GaAs as shown in **Fig. 3**(**b**). The TEM image shows a smooth HfO_2/GaAs interface with no significant amount of defects present and also indicates the formation of a high quality gate dielectric layer of thickness 6 nm. According to the HRTEM, HfO_2 shows polycrystalline, which increases leakage current. It is worth to note that the interface properties and leakage current can be improved significantly by using interface passivation layer, alloy dielectric, and plasma nitridation of the dielectric [**34-44**]. In order to further verify accuracy of the models used, a MOSFET has been simulated using the process recipe followed by Kim *et al.* [**9**] and the output characteristics have been compared and plotted in **Fig. 3**(**c**). It is observed that the simulated results are well in accord with the experimental results.

The output characteristics $(I_D - V_D)$ of GaAs MOSFET with 6 nm HfO_2 gate dielectric layer with different effective channel lengths (L_{eff}) of 100 nm, 60 nm, 40 nm, 30 nm and 20 nm at a gate voltage of 2.2V are shown in **Fig. 4**(**a**). A maximum drive current of ~1.3 mA/μm is obtained for L_{eff} = 20 nm and drain bias of 1.5V. This is attributed to the higher channel mobility and superior HfO_2/GaAs interface as reported previously [**27**]. It can be seen that the drain current increases almost linearly for small biases and then it tends to saturate. However, a very close inspection to the curves shows that even in saturation region the drive current increases gradually. Such gradual increase of drive current is attributed to the channel-length modulation effect, a consequence of several short-channel effects. Such increase in current can be parameterized by a channel length modulation factor λ as [**45, 46**]:

$$I_D = I_D'(1+\lambda V_D) \tag{6}$$

where, I_D' is the drain current without channel length modulation. When the current is extrapolated backward from saturation region, it meets the V_D-axis (i.e. $I_D = 0$) at $V_{DS} = \frac{1}{\lambda}$ [**45**]. For an ideal MOSFET, λ is zero and current does not increase with increasing drain voltage after the saturation is reached. The λ values for the MOSFET of current consideration are extracted to be 0.067, 0.047, 0.045, 0.043, 0.04 V^{-1} for L_{eff} values of 100, 60, 40, 30 and 20 nm, respectively and thereby the values imply very insignificant short-channel effect.

Fig. 4(**b**) shows the variation of drain current (I_D) with gate overdrive voltage (V_G -V_{TH}) of the GaAs MOSFETs of different L_{eff} at a drain bias of 1.5V. Excellent sub-threshold characteristics are exhibited for all channel lengths and on-state to off-state current ratio (I_{on}/I_{off}) of 12 orders of magnitude is also achievable.

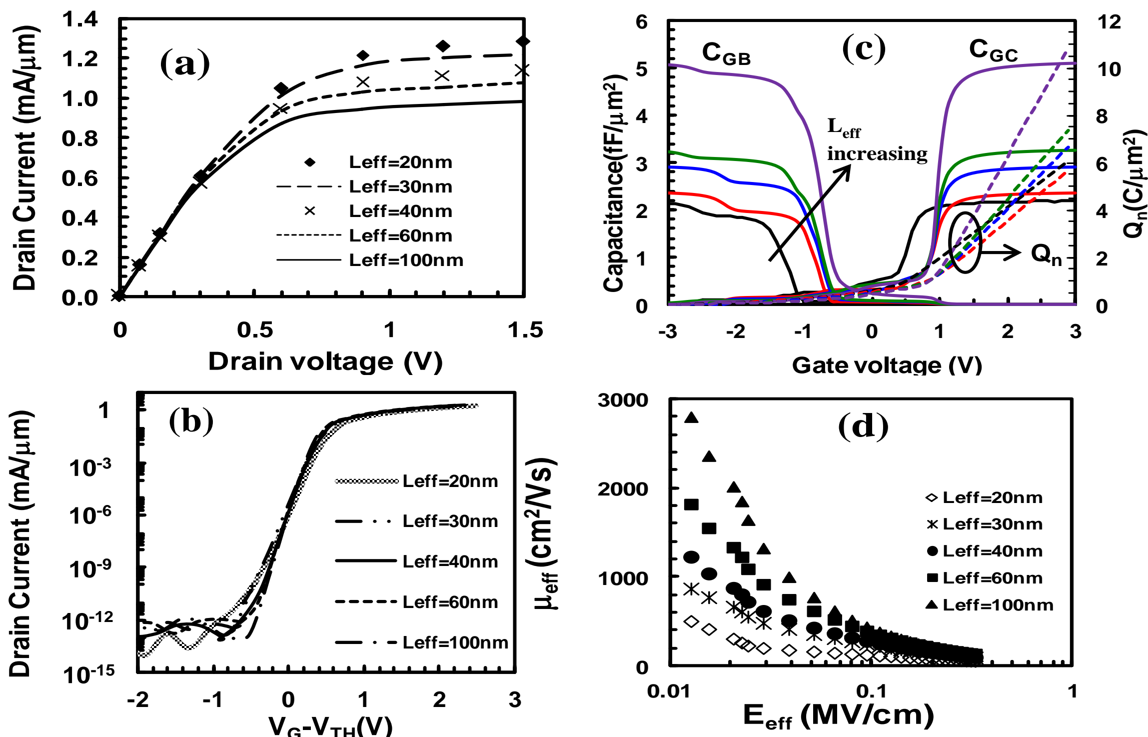

Fig. 4. (a) Output characteristics for various channel lengths at gate bias of 2.2V. (b) Transfer characteristics for various channel lengths at drain bias of 1.5V. (c) Plots of variation of simulated gate-to-body (C_{GB}) and gate-to-channel (C_{GC}) capacitance values, keeping in mind the split C-V measurement technique. It also includes the estimated inversion charge (Q_n) with gate bias. (d) Effective carrier mobility as a function of effective electric field.

Fig. 4(**c**) shows the variation of estimated gate-to-body (C_{GB}) and gate-to-channel (C_{GC}) capacitance values and relevant inversion charge (Q_n) with gate bias. Such simulation is performed by considering the split C-V measurement technique. Once Q_n is obtained, the effective mobility can be obtained as [**46**]:

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$$\mu_{eff} = \frac{g_d L_{eff}}{Q_n W} \quad (7)$$

where, g_d is the output conductance, L_{eff} is the effective channel length and W is the channel width.

The variation of effective mobility (μ_{eff}) with effective electric field in the channel is shown in **Fig. 4**(**d**). A maximum effective mobility of 1200 cm^2/Vs has been obtained which is higher than the previously reported values of 560 cm^2/Vs [**47**], 570 cm^2/Vs [**48**] and 970 cm^2/Vs [**9**].

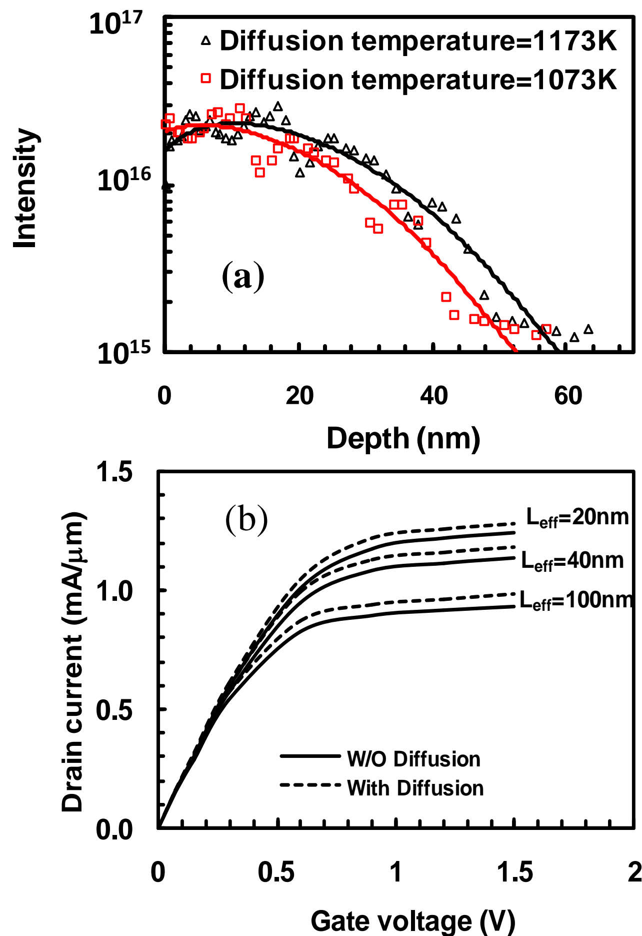

Fig. 5. (a) Intensity of oxygen diffusion from the HfO_2/GaAs interface into the substrate for different annealing temperatures of 973K and 1073K; (b) Comparison of output characteristics with (dashed lines) and without (solid lines) the effect of oxygen diffusion.

The amount of oxygen diffusion from HfO_2 layer through the interface into the GaAs substrate for annealing temperatures (T_{anneal}) of 700 ^{O}C and 800 ^{O}C, relevant for MOS processing, is shown in **Fig. 5**(**a**). It is apparent that there is a significant amount of oxygen diffusion during processing and the extent of diffusion tail increases with thermal budget. Consequently, the diffused oxygen will alter the effective doping profile of the device thereby changing its electrical characteristics. **Fig. 5**(**b**) shows the effect of such oxygen diffusion on electrical characteristics of the MOSFETs at an annealing temperature of 1073K. The plots indicate that there is 3-5 % enhancement in drain current in presence of diffusion. This is attributed to the fact that oxygen is an n-type dopant to GaAs and the diffused oxygen effectively increases net doping of the channel.

The effect of oxygen diffusion on the device performance parameters such as threshold voltage, transconductance and DIBL is shown in **Fig. 6**. The device speed (v_0) has also been calculated for MOSFETs with and without diffusion using the following expression [**49**];

$$v_0 = \frac{g_m}{WC} \quad (8)$$

where, g_m is transconductance, W is width of the device and C corresponds to the gate-to-channel capacitance per unit area [**49**].

It is observed that oxygen diffusion has adverse effects on DIBL. This is attributed to the fact that oxygen, due to its high reactivity, forms deep carrier traps in the GaAs bandgap [**50**]. On the other hand, improvement in transconductance and threshold voltage is observed which is due to the increase in drain current.

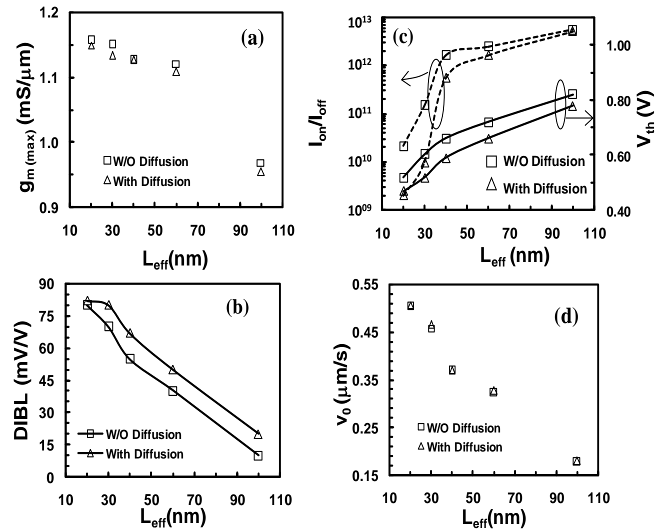

Fig. 6. (a) Transconductance; (b) DIBL; (c) Threshold voltage and current ratio; and (d) Device speed for various channel lengths with and without the effect of oxygen diffusion.

Conclusion

The HfO_2/GaAs MOS capacitors have been fabricated and characterized. A process recipe for virtually fabricating GaAs channel MOSFETs with HfO_2 gate dielectrics has been developed and its electrical performance is obtained by simulating the structure with input data obtained from the experimental MOS capacitors. Several parameters such as flat band voltage, oxide thickness, interface state density, fixed oxide charge, and doping concentration are extracted and fed into the simulator. The electrical characteristics have been observed. Also, the effect of oxygen diffusion, from the oxide into the substrate, on the electrical parameters has been studied. It is noted that oxygen diffusion has adverse effect on DIBL but at the same time improves transconductance and threshold voltage of the HfO_2/GaAs MOSFET devices.

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Author contribution

Conceived the plan: A.D., S.C., G.K.D.; Performed the experiments: A.D., G.K.D.; Data analysis: A.D., S.C.; Wrote the paper: A.D., S.C., G.K.D. Authors have no competing financial interests.

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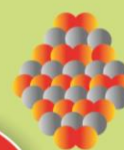

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