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Effect of diffusion parameters on the efficiency of c-Si solar cell

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ABSTRACT

This paper presents the effect of emitter thickness and post-annealing process on the conversion efficiency of crystalline silicon (c-Si) solar cells. Diffusion parameters like pre-deposition temperature, drive-in temperature, and process duration assist to control the emitter thickness and inturn improves the conversion efficiency of the solar cells. It is observed that shallower emitter cells have higher conversion efficiency of 10.81% than deeper emitter cells of 7.62%. Post-annealing process at 700°C for 60 minutes boosts the efficiency of shallower emitter cell from 10.81% to 12.06%. Dark current-voltage characteristics authenticate the formation of p-n junction and also elucidate the presence of recombination saturation current along with diffusion saturation current. Illuminated and dark current-voltage characteristics further provide the evidence that post-annealing process during phosphorus diffusion reduces the trap density and thus the recombination saturation current, which helps to improve the efficiency. The combination of a shallower emitter with post-annealing process provides an excellent approach to enhance the solar cell efficiency. Copyright © 2015 VBRI Press.

Keywords: Semiconductor; p-n junction; diffusion; solar cell; X-ray diffraction.

Introduction

In present time, there has been a great deal of interest in renewable-energy sources. This has been partially prompted by the increase in petroleum prices worldwide as a consequence of geopolitical and economic elements. Of all the available energy sources, photovoltaic is perhaps the best way to meet all the future requirements. Crystalline silicon (c-Si) is one of the most promising candidates for photovoltaic application due to its optimum band gap of 1.12 eV for AM 1.5 solar spectrum, small ionic impurities, low moisture absorption, high UV stability, wide operating temperature range and excellent electrical insulating properties **[1-10].** The junction fabrication, either n-type or p-type, is easier and very precisely controllable in silicon, which further makes it beneficial for photovoltaic application **[1].** In p-n junction solar cells, p-type or n-type silicon can be used as the base. However, p-type silicon is preferred as the base due to its better minority carriers transport characteristics **[1, 2].** In solar cells, p-n junction provides the spatial asymmetry (asymmetry in resistance) which is essential for charge carrier separation. This junction acts as a selective barrier for transportation of charge carriers and provides the low-resistance path for electrons to the n contact and holes to the p contact **[1, 2].** Junction depth (emitter thickness) is the crucial parameter in the Si solar cells. This is fabricated by either ion implantation or diffusion method. Nevertheless, the diffusion process preferred over Ion implantation because it doesn't create any crystal damage and also provides higher-quality junction with a minimum leakage current **[11-13].** Two step diffusion processes preferred for fabrication of p-n junction in which the first step of the diffusion process deposits the PSG glass (phosphor silicate glass) on silicon, which further serves as a source for subsequent phosphorus diffusion. Junctions made by the diffusion process are governed by the diffusion parameters like temperature, process duration, and flow rate of $POCl_3$, etc. Diffusion occurs at all temperatures, but this has a strong dependence on temperature because of diffusivity which itself has an exponential dependence on temperature **[11, 12].** The aim of this work is to investigate the effect of different phosphorus diffusion parameters like pre deposition temperature, drive-in temperature, and process-duration on the emitter thickness and thus on the conversion efficiency of the solar cells. Further, this study observes the impact of post annealing process during phosphorus diffusion on the life-time of minority charge carriers. Experimental results provide the evidence that shallower emitter has better performance. The combination of shallower emitter with post-annealing process provides a new path to improve the solar cell efficiency.

Experimental

Materials

Czochralski grown, 270 μm thick, P-type Si wafers (Boron doped, sheet resistance 24.3 Ohm/square) were used for this work. These prime grade wafers were purchased from

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Wafer World, Inc., USA. Other chemicals as hydrochloric acid (HCl), ammonium hydroxide (NH4OH), hydrogen peroxide (H_2O_2), buffered oxide etch solution (BOE), and hydrofluoric acid (HF) were Cleanroom® MB GRADE and obtained from Electronic Chemical, Inc., USA. Photoresist AZ5214E was supplied by AZ Electronic Materials, USA and developer MF-26 was delivered by Microposit® MF 26 Developer, USA.

Methods

All wafers were chemically cleaned using a standard procedure and then dipped in the diluted HF solution before inserting in an oxidation furnace. A thick oxide (SiO_2) layer of 1080 nm was grown on front and back surfaces of the wafer by the wet oxidation method at 1100 °C. This oxide layer acts as a mask during phosphorus diffusion for back surface. The presence of SiO_2 layer among cells made them isolated from each other. The fabrication details are shown in **Fig. 1**.

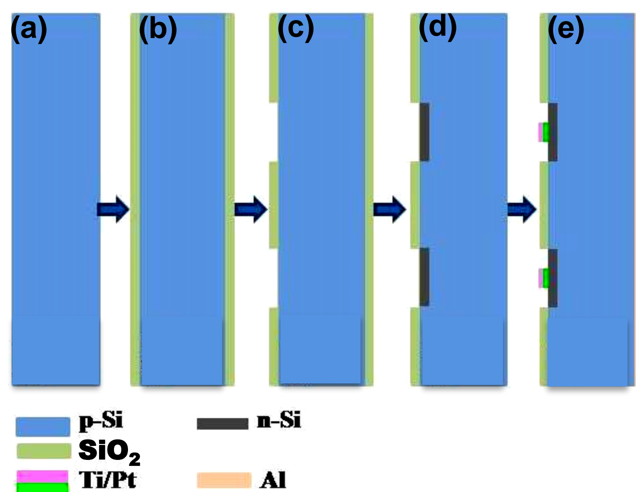

Fig. 1. Different fabrication steps of the solar cells: (a) Initially RCA cleaned p-Si wafer, (b) 1080 nm SiO_2 deposition, (c) device area opening using optical lithography, (d) phosphorus diffusion and back side SiO_2 removal, (e) Ti/Pt front electrode and Al back electrode deposition and finally forming gas annealing at 450 °C for 30 minute.

Table 1. Details of the diffusion parameters of the solar cells.

Device group Name	Pre-Deposition Temp(°C)/Time (Min)	Drive-in Temp(°C)/Time (Min)	Post-annealing Temp(°C)/Time (Min)	Junction Depth (μm)
A	850 / 30	950 / 30	-	0.453
B	850 / 30	950 / 30	700 / 60	0.453
C	1000 / 15	1000 / 45	700 / 60	1.151

Highly doped n^+-emitters were formed by phosphorus diffusion using a $POCl_3$ liquid as a phosphorus source at different temperatures. The details of the devices with their pre-deposition temperature, drive-in temperature, and process-duration are given in **Table 1** under three groups A, B, and C. Each group has five devices. The phosphor-silicate glass formed during the phosphorus diffusion was removed by BOE solution. Selective front electrode patterns of Ti/Pt (titanium / platinum) were fabricated by lift-off technique while the blanket aluminum (Al) film was deposited for back electrode. Forming gas annealing (N_2: H_2: 9: 1) at 450 °C for 30 minutes was used to amend the contact quality. The devices fabricated as per the literature **[14].**

Solar cell efficiency was calculated using Oriel Sol3A class AAA solar simulator (model 94023A) under AM1.5 G spectral irradiance (100mW/cm^2 at 25°C). Dark I-V characteristics and diode transient characteristics were measured by semiconductor device parameter analyzer (model no. B1500A). EVG double sided mask aligner, model no. 610, was used for optical lithography. Electrode deposition was carried out in a Techport Sputter coater system. High Resolution X-ray diffraction (HRXRD) measurements were done by the Rigaku smart lab system using CuK_α (λ=1.54Å) as X-ray source. Doping profile and junction depth were estimated by the ATHENA process simulator.

Results and discussion

Table 1 shows the effect of different doping parameters on n^+-emitter thickness (junction depth). The junction depths of samples A, B, and C are 0.453, 0.453, and 1.15 microns respectively. Gaussian model has been applied to calculate the junction depth **[11, 12].** Diffusion parameters confirm that shallow junction is formed at lower temperatures while higher temperatures are required to form the deeper junction. Fick's second law of diffusion explains the relation between temperature, process- duration, junction depth, and dopant concentration **[11, 12].**

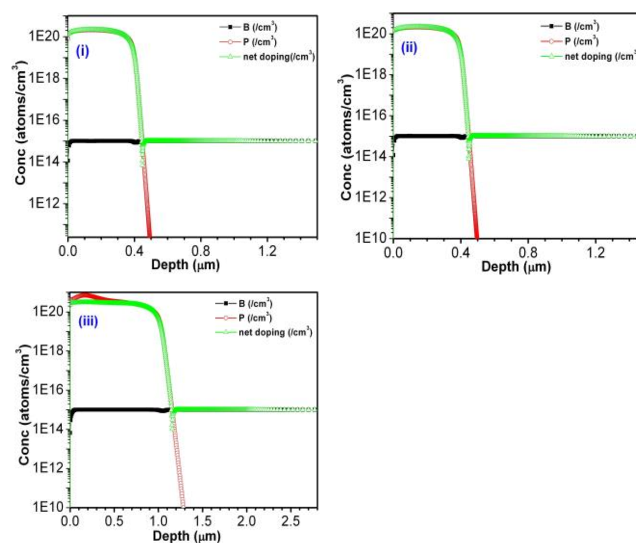

Fig. 2. Doping concentration versus junction depth profile of solar cells belongs to the (i) group A, (ii) group B, and (iii) group C by ATHENA process simulation.

Fig. 2 represents the plot of doping profile versus junction depth for different samples and reveals that doping concentration is maximum at the surface while, declining with depth and finally at the end of the junction, doping concentration becomes equal to the substrate concentration. This affirms the non-uniform doping in the n+-region. It also reveals that doping profile contains three regions- (i)

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surface region, (ii) kink region and (iii) tail region. The incorporation of P atoms in the Si governs through the interstitialcy diffusion mechanism which involves the dissimilar types of vacancies. Vacancies are always present inside the crystal. However, their concentration varies with temperature and dopant concentration. Doped samples have more vacancies than undoped samples. The detail of vacancy and interstitial is discussed in the literature **[2]**. In the diffusion process, when phosphorus atoms enter on the surface, some fraction of atoms is paired with doubly ionized vacancies (V=) through the reaction $P^+ + V^= = P{+}V^=$. This mechanism is dominated only in the surface region, which is flat, while the kink region starts where the P diffusivity becomes dominated by excess $P{+}V^-$ formation. The dissociation of $P{+}V^=$ pair into $P{+}V^-$ pair and an electron state occur in the steeper region of the curve, but they do not dissociate significantly until the Fermi level position reached to just 0.11eV below the conduction band.

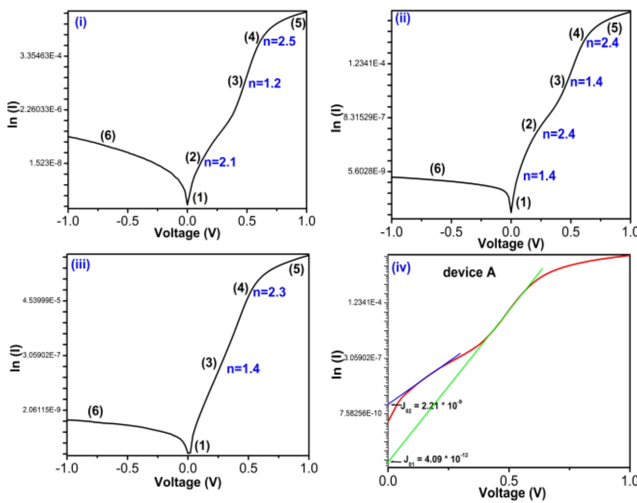

Fig. 3. Dark I-V characteristic of (i) device A, (ii) device B, (iii) device C and (iv) Calculation of J_{01} and J_{02} currents from the dark I-V of device A.

Fig. 3 (i, ii, iii) shows the dark I-V characteristics of different solar cells and confirms the formation of p-n junction. Total current (I) is expressed as **[15-17]:**

$$I = I_{DIFF} + I_{R\text{-}G} \quad (1.1)$$

$$= I_0(e^{qV/kT} - 1) + qAn_iW(e^{qV/2kT} - 1)/2\tau \quad (1.2)$$

$$I_0 = qA[(D_n N_i^2/L_n N_A) + (D_p n_i^2/L_p N_D)]$$

where $\mathbf{I_{DIFF}}$ is the diffusion current, $\mathbf{I_{R\text{-}G}}$ is the recombination generation current, I_0 is the reverse saturation current, q is the electronic charge, V is the applied voltage, k is Boltzmann constant, T is temperature, A stands for the area of device, D is the diffusion coefficient, L is the diffusion length, N_i is the intrinsic carrier concentration, N_A is acceptor concentration, N_D is donor concentration, W is the depletion width, and τ is the effective life-time of charge carrier. In **Fig. 3**, current does not follow the ideal I-V characteristics of the p-n junction diode. This deviation is explained on the basis of ideality factor (n), which is expressed as **[15-17]:**

$$n = (1/26{*}10^{-3}){*}(V_1 - V_2)/\ln(I_1/I_2) \quad (2)$$

where, I_1 is the current corresponding to the voltage V_1. Various values of ideality factor are mentioned in the **Fig. 3**. These values of ideality factors explain the contribution of different dominant mechanism in various regions of the dark I-V curve. Details of different regions [(1), (2), (3), (4), and (5) in forward bias and (6) in reverse bias] in I-V curve and their corresponding dominant mechanism are given in the **Table 2.** In forward and reverse bias, I-V curve deviates from the ideal p-n junction characteristics due to presence of $\mathbf{I_{R\text{-}G}}$ as an additional component of current along with diffusion current. In Si p-n junction diode at room temperature, $I_{R\text{-}G}$ dominates at reverse biases and small forward biases (n=2 region at lower voltage).

Table 2. Dominant mechanism corresponding to various regions of dark I-V.

Region No.	Ideality Factor (n)	Dominant Mechanism
1	-	Shunt resistance effect
2	2	Recombination of carriers in the depletion region
3	1	Diffusion saturation current
4	2	High level injection
5	-	Bulk and/or contact resistance
6	-	Generation of carriers in the depletion region

Region (1), in **Fig. 3**, deviates from the ideal p-n junction I-V characteristics due to the presence of lower shunt resistance in comparison to the ideal p-n junction which has nearly infinity shunt resistance. The value of shunt resistance can get from dark I-V as well as from illuminated I-V (**Fig. 4**) **[15-17].** Amid all the devices, device B has lower shunt resistance than others.

Region (2), in **Fig. 3**, comes due to recombination of the charge carriers in the depletion region and provides an additional recombination current along with diffusion current. In forward bias, carrier concentration in the depletion region is more than their equilibrium value, i.e. $NP > N_i^2$ [N = equilibrium electron's concentration, P= equilibrium holes concentration, and N_i= intrinsic level concentration (10^{10} atoms/cm^3) at T=300 °C for Si] which leads the thermal recombination of charge carriers throughout the depletion region. Anytime an electron and hole recombine anywhere within the diode, one electron flows in the external circuit and participates in the current. The presence of several trap states inside the band gap motivates the recombination. The presence of a region (2) at lower voltage in the forward bias is explained by two diode model.

The details of two saturation currents J_{01} (diffusion saturation current) and J_{02} (recombination saturation current) are given in **Fig. 3**(**iv**) and in **Table. 3**. **Table 3** and **Fig. 3**(**iv**) confirms the higher value of J_{02} than J_{01} in the lower voltage region and follows the reverse trend in the higher voltage region. Different impact of J_{01} and J_{02} in various voltage regions comes due to different ideality factors corresponding to J_{01} (n=1) and J_{02} (n=2).

Table 3 confirms the lower value of J_{02} of device B than A due to annealing effect. As, recombination life-time of the charge carriers is inversely proportional to the trap density, hence the presence of higher trap density reflects

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the lower recombination life-time of charge carriers as well as higher recombination losses. Annealing reduces the trap density and hence improves the life-time of charge carriers, which reduces the recombination losses in the device. Recombination current (I_{R-G}) is always present along with diffusion current in the forward bias, but at higher voltage region, recombination current is only a small fraction of the total current, thus it is negligible. The absence of the region (2) in **Fig. 3**(**iii**) indicates the insignificant recombination losses in the device C. This too brings out the lowest trap concentration in the device C in comparison to other devices A and B. This result is further supported by XRD measurement.

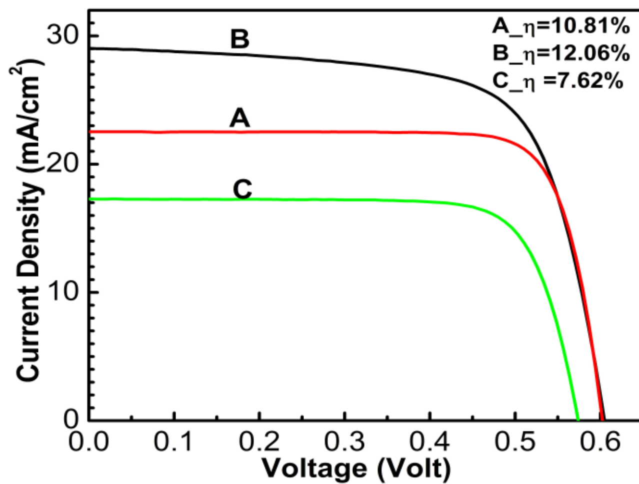

Fig. 4. I-V characteristic of the best solar cells (3,2*3.2 mm^2) of group A, B and C under illumination.

Table 3. J_{01}(diffusion saturation current) and J_{02}(recombination saturation current) currents corresponding to the devices of groups A, B and C.

Device Name	J_{01} (A)	J_{02} (A)
A	$4.09*10^{-12}$	$2.21*10^{-9}$
B	$3.98*10^{-11}$	$7.73*10^{-10}$
C	$8.37*10^{-11}$	0

Region (3), in forward bias, shows the ideal diode characteristics due to presence of the unit ideality factor. The existence of a straight line in the natural log graph confirms the exponential dependence of current on voltage. The presence of a longer region (3) in the dark I-V corresponds the superior solar cell with good-quality p-n junction. Among devices A and B, B has been longer n=1 region and hence this has better efficiency. However, the longest n=1 region is present in the device C, but due to higher junction depth, this has least efficiency. A good-quality p-n junction can fabricate at any depth, but for good-quality c-Si solar cell, it should be ordered of 0.5 micron **[1].**

Region (4), having the ideality factor n=2, reveals the high level injection phenomena in forward bias, i.e. ΔN, $\Delta P >> N_i$, where ΔN, ΔP is excess electrons and holes. In forward bias, the largest minority concentration occurs at the depletion region edges. At high level injection, the excess minority concentration approaches the majority concentration and the minority carrier assumption completely gone because of very high concentration of both the charge carriers. If the bulk region is to maintain charge neutrality, the majority carrier concentration has also increased significantly above its equilibrium value. The deviation of an ideality factor from unity reduces the solar cell efficiency.

Region (5), in **Fig. 3**, correspond the bulk region effects or series resistance effect and can be discussed on the basis of change in Fermi levels. Fermi levels corresponding to the electrons (F_n), and holes (F_p) are considered as flat throughout the depletion region in low current levels in the forward bias. While at higher current levels, this is not flat. The Fermi levels are dropping or deviating from their flat position. These drops are given by ΔF_n and ΔF_p for electrons and holes respectively. Now the equation of total dark current is modified and written in the form **[17]:**

$$I=I_0\,(e^{[qV - \Delta Fn - \Delta Fp]/kT} - 1) + I_{R-G} \tag{3.1}$$

$$\Delta F_n = J_n * R_{series} \tag{3.2}$$

$$\Delta F_p = J_p * R_{series} \tag{3.3}$$

where J_n and J_p are the current corresponding to the electrons and holes respectively. R_{series} is the series resistance of the device and expressed as the sum of base resistance, emitter resistance, front electrode resistance, and back electrode resistance. At low current levels, there is no significant voltage drop in the bulk, thus applied voltage is equal to the voltage across the depletion region. While, at high-current levels, bulk resistance can produce a significant voltage drop ($J*R_{series}$) in the bulk region, and thus the applied voltage is larger than the voltage across the depletion region. This voltage drop in the bulk region produces the significant value of ΔF_n and ΔF_p, which causes the deviation in I-V characteristics from the ideal diode characteristics in the higher current regions. When the current density is quite larger, either high level injection or the series resistance of the device, or both, becomes significant. High level injection has the effect of changing the ideality factor about two. The series resistance increases the voltage drop across the diode for a given current. Slopes (dV/dI) at the higher voltage region in **Fig. 3** (i, ii, iii) confirm the existence of nearly equal series resistance in all the devices. This is further verified by the illuminated I-V characteristics (**Fig. 4**).

Region (6), in **Fig. 3**, reveals the presence of generation current due to the generation of the charge carriers in the depletion region. In reverse bias when the carrier concentration in the depletion region is reduced below their equilibrium value, i.e. $NP < N_i^2$, leads to the thermal generation of electrons and the holes throughout the depletion region. The presence of higher electric field in the depletion region swept the generated carriers into the quasi neutral regions, thereby adding to the reverse current. Anytime an electron and hole generate anywhere within the diode, one electron flows in the external circuit and

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participates in the current. For ideal diode, in reverse bias, current saturates at lower voltages. Whereas in the real diodes, reverse current increases with applied voltage due to presence of recombination-generation current (I_{R-G}). This recombination-generation current is proportional to the depletion width or square root of applied voltage and written as;

$$I = -I_0 - qAN_i\,W/2\tau \quad (4)$$

$$= -(I_0 + qAN_i\,W/2\tau) \text{ or } I \propto (V_{bi} - V_A)^{1/2}$$

where V_A has negative value due to reverse bias and V_{bi} stands for built in bias voltage. Various amplitudes of currents in the region (6) in devices A, B, and C reflect the different generation life-time of the minority charge carriers in different devices and confirm that Device A has least generation life-time of minority charge carriers due to presence of maximum recombination-generation current. For device B and C, the currents in the region (6) are nearly comparable and hence the generation life-times of minority charge carriers are nearly equal. Annealing improves the generation life-time of minority charge carriers and hence reduces the generation current in device B than A.

Table 4. Different solar cell parameters of the devices of groups A, B, and C. Symbols have their usual meanings.

S. NO.	Device group Name	Voc (Volt)	Jsc (mA-cm^{-2})	FF	η (%)
1	**A**	0.601	21.89	79.69	10.48
2		0.600	22.18	79.67	10.62
3		0.600	22.51	79.61	10.76
4		0.601	22.52	79.86	**10.81**
5		0.600	22.48	78.81	10.64
6	**B**	0.603	27.91	70.28	11.83
7		0.601	30.93	63.31	11.78
8		0.604	29.02	68.83	**12.06**
9		0.602	30.20	64.95	11.82
10		0.604	27.62	69.07	11.52
11	**C**	0.574	15.74	79.54	7.20
12		0.575	15.52	79.53	7.09
13		0.562	15.85	76.94	6.86
14		0.573	17.27	77.05	**7.62**
15		0.575	15.53	76.90	6.82

Fig. 4 shows the illuminated I-V characteristics of the solar cells and **Table 4** represents their corresponding parameters. Solar cells of group A, B, and C show the best efficiency of 10.81%, 12.06% and 7.62% respectively. This confirms the better performance of shallow emitter solar cells A and B. A moderately dope emitter cell prefers over very thin and thick emitter cells due to its lower series resistance as well as Auger recombination losses. Very thin junction provides the higher series resistance while deep junction creates some detrimental problems, which reduce the performance of solar cell **[1].** At AM1.5 Solar spectrum most of the intense light falls in the region of 480 nm to 580 nm and their corresponding absorption length is nearly 1 µm. When the junction depth is more than 1 µm the most intense light is absorbed in the highly doped region, which provides the higher scattering and recombination centers. Due to high scattering the large fraction of the generated charge carriers recombine before reaching their respective electrodes and thus reduces the conversion efficiency **[1, 18].** The conversion efficiency is also affected by the presence of dislocations and contaminates like C, O and Fe in the wafer. In c-Si wafer lattice site density is $5*10^{22}$ cm^{-3} while most of the Cz-Si wafers have C and O density more than 10^{16} cm^{-3}. The presence of C and O creates several trap states and recombination centers in the band gap which reduces the solar cell performance **[1, 2].** Metal impurities also generate some detrimental problem in the device due to their higher diffusivity in Si than dopant phosphorus **[1, 2].**

Table 4 indicates the lower open circuit voltage of device C due to the lower current density. **Table 4** also exhibits that annealed samples of device B have better efficiencies than unannealed samples of the device A. Annealing helps to eliminate the dislocations which reduce the trap centers and as well as recombination losses and hence boost the short circuit current density in the samples of the group B. This is further confirmed by using X-ray diffraction patterns of devices. High resolution symmetric and asymmetric XRD measurements have been performed to analyze the isotopic/anisotropic nature of the strain induced due to different diffusion parameters of devices.
Introduction of phosphorus atoms in the Si wafer generate stresses due to different radii of phosphorus (1.07Å) and silicon (1.17Å). This results the tensile stress in the diffused layer while compressive stress in the undiffused substrate. The amount of stress generation in the devices is the function of surface concentration as well as the junction depth **[19]**. **Fig. 5** (**i**) shows the symmetric XRD patterns of doped and undoped samples. This confirms the single crystalline silicon substrate has (100) orientation due to presence of diffraction peak near 69.10°. To measure the X-ray diffraction pattern of (111) crystallographic orientation, asymmetric XRD has been done. **Fig. 5** (**ii**) shows the asymmetrical XRD pattern of different samples at (111) crystallographic orientation. In XRD measurement, the diffraction vector (a vector that bisects the angle between the incident and diffracted beam) and the normal vector of the plane should be parallel.

As the orientation of normal vectors of (100) and (111) planes are different, so to measure the asymmetric XRD pattern of (111) plane, the sample is tilted by an angle 54.74° with respect to normal of the plane (100) to make sure the both vectors (diffraction vector and normal of the (111) plane) are parallel **[20]**. **Fig. 5** shows the shifting of the XRD peaks is different in both patterns. This is due to generation of asymmetrical (anisotropic) stress inside the samples **[21]**. Thus, shifting of XRD peaks clearly specifies about the variation in defect density in different devices. These variations in XRD peaks are explained by Bragg's law. The Bragg's diffraction law is expressed as **[22]**:

$$2\, d_{hkl} \sin\theta_B = n\lambda$$

where d_{hkl} is the inter planer spacing, n is the order of diffraction, λ (CuKα = 1.54 Å) is the X-ray wavelength, and θ_B is the Bragg's angle. Bragg's diffraction angle (θ_B) depends only on the inter planer spacing for fixed n and λ. This has smaller value for higher dhkl, and larger value for lower d_{hkl}. The variation in stress decides the deviation in

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dhkl. If the stress is tensile, dhkl will be more and hence, θ_B will be smaller. The reverse is true for compressive stress. XRD patterns reveal the sample A, which is unannealed after P diffusion, has more strain in comparison to annealed sample B, while, amid B and a C sample, C has the lesser strain than B. The efficiency of the devices A and B follows the same pattern while sample C has a lesser efficiency even it has the least strain. Device C has least efficiency due to the presence of higher junction depth than devices A and B. Dark I-V characteristics of the devices follow the same pattern.

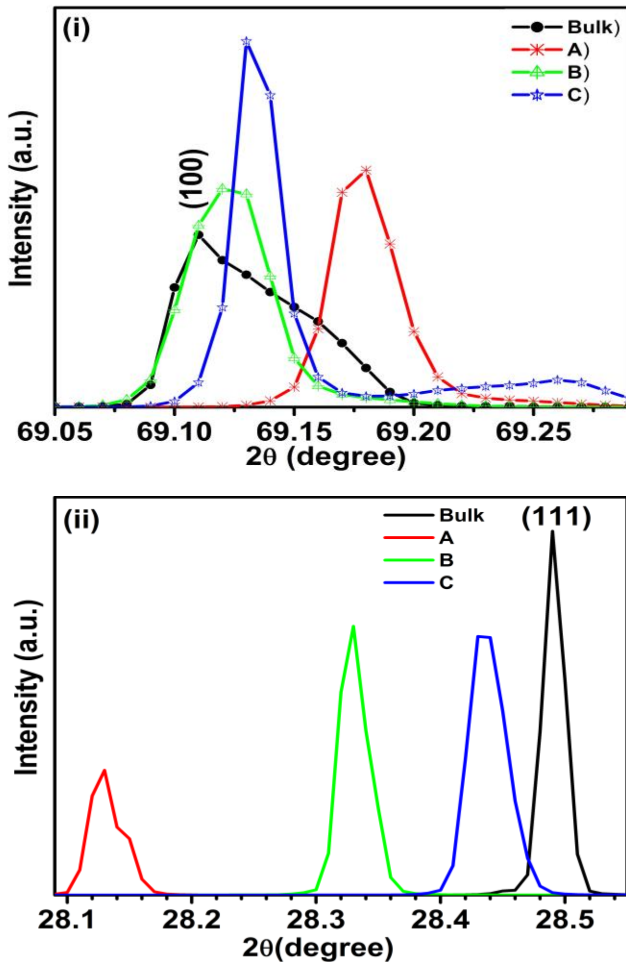

Fig. 5. (i) Symmetric XRD of devices A, B, C and bulk Si along (100) direction, (ii) Asymmetric XRD of devices A, B, C and bulk Si along (111) orientation.

Fig. 6 indicate the diode transient characteristics of the devices. The storage delay times of devices A, B, and C are 0.632 μ-second, 2.396 μ-second, and 2.173 μ-second respectively. The relation of storage delay times with life-time of minority charge carriers in n^+-p junction is written as **[15-17]:**

$$t_{sd} = \tau * \ln(1+I_f/I_r) \quad (5)$$

where t_{sd} = storage delay times, I_f = forward saturation current, I_r = reverse saturation current, and τ = minority charge carrier life-time.

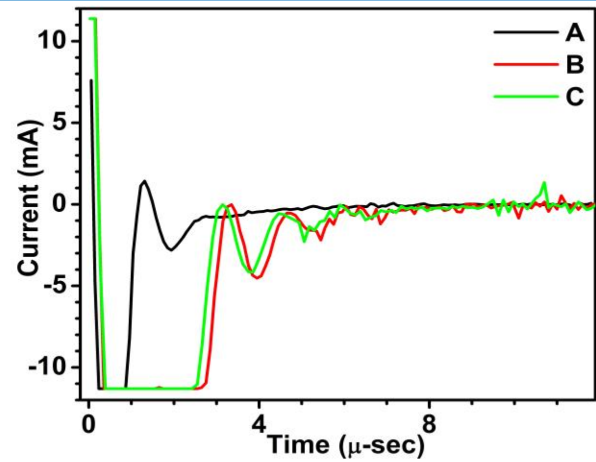

Fig. 6. Diode transient characteristics of solar cells belong to group A, B, and C.

As the storage delay times are proportional to the life-time of the minority charge carriers, hence, the life-times of minority charge carriers are least in device A and nearly equal in devices B and C. This result is earlier authenticated from the dark I-V characteristics as well as by Illuminated I-V characteristics. The symmetrical and asymmetrical XRD patterns earlier confirm that device A has the higher strain in comparison to B and C, so this might reduce the life-time of the minority charge carrier in the device A.

Conclusion

The impact of diffusion parameters, emitter thickness, and post-annealing process on conversion efficiency of c-Si solar cells is demonstrated. A shallower emitter of 0.453 microns is formed at a low diffusion temperature, while, the fabrication of a deeper emitter of 1.153 microns requires a comparatively high diffusion temperature. The emitter thickness plays a key role to decide the cell efficiency. Shallower emitter cells have better conversion efficiency of 10.81% than deeper emitter cells of 7.62%. Shallower emitter cells have also an excellent open circuit voltage than thicker emitter cells due to the higher short circuit current accessibility. Post-annealing treatment at 700 °C for 60 minutes further enhanced the efficiency of shallower emitter cell from 10.81% to 12.06% by cutting back the trap density. The annealing process minimized the recombination saturation current in forward bias and generation current in reverse bias and thus improved the life-time of minority charge carriers. This study develops a new approach to boost the solar cell efficiency.

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